3850 Group (Spec. H)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3850 group (spec. H) is the 8-bit microcomputer based on the 740 family core technology.

The 3850 group (spec. H) is designed for the household products and office automation equipment and includes serial I/O functions, 8-bit timer, and A-D converter.

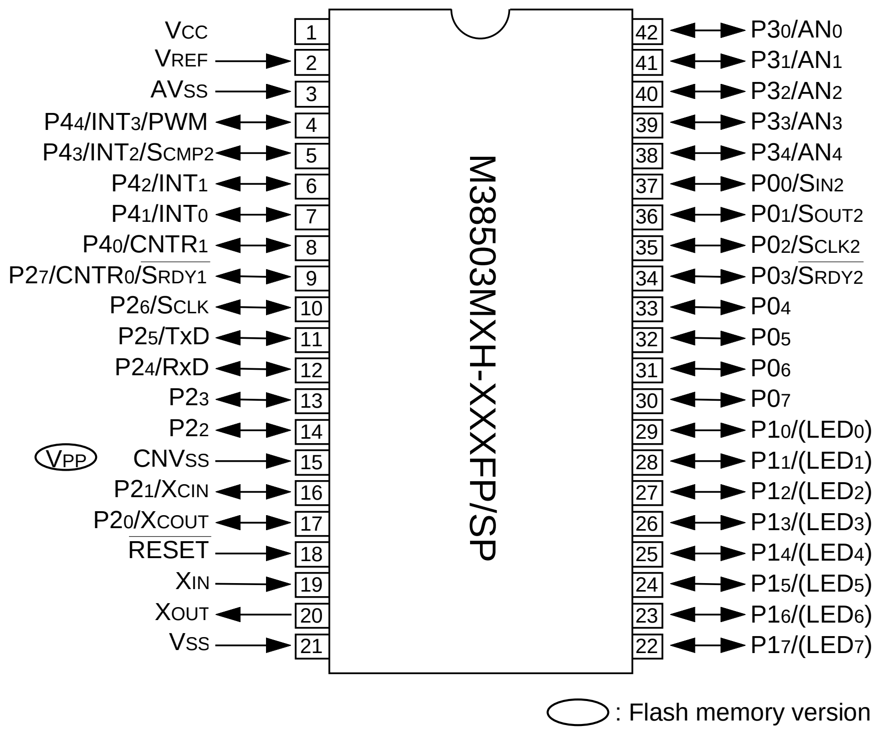
FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time .... 0.5 µs (at 8 MHz oscillation frequency)
- Memory size
  - ROM .... 8K to 32K bytes
  - RAM .... 512 to 1024 bytes
- Programmable input/output ports 34
- Interrupts .... 15 sources, 14 vectors
- Timers .... 8-bit × 4
- Serial I/O1 .... 8-bit × 1(UART or Clock-synchronized)
- Serial I/O2 .... 8-bit × 1(Clock-synchronized)
- PWM .... 8-bit × 1
- A-D converter .... 10-bit × 5 channels
- Watchdog timer .... 16-bit × 1
- Clock generating circuit..................................... Built-in 2 circuits (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  - In high-speed mode .... 4.0 to 5.5 V (at 8 MHz oscillation frequency)
  - In middle-speed mode .... 2.7 to 5.5 V (at 8 MHz oscillation frequency)
  - In low-speed mode .... 2.7 to 5.5 V (at 32 kHz oscillation frequency)
- Power dissipation
  - In high-speed mode ....34 mW (at 8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode .... 60 µW (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ....–20 to 85°C

APPLICATION

Office automation equipment, FA equipment, Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : FP .... 42P2R-A/E (42-pin plastic-molded SSOP)
Package type : SP .... 42P4B (42-pin plastic-molded SDIP)

Fig. 1 M38503MXH-XXXFP/SP pin configuration

FUNCTIONAL BLOCK

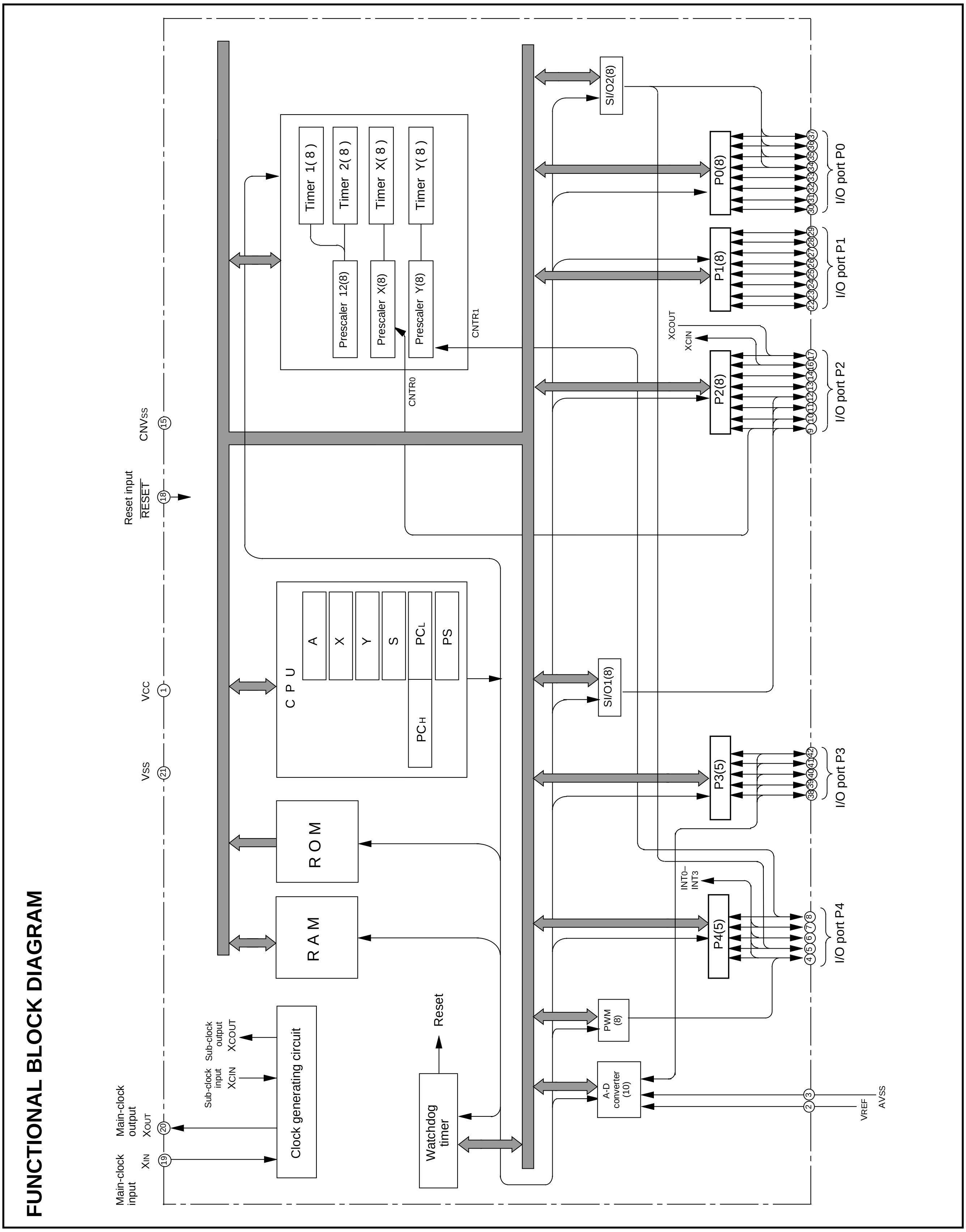


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Functions	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss.	
CNV_{SS}	CNV_{SS} input	•This pin controls the operation mode of the chip. •Normally connected to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active “L.”	
X_{IN}	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0/S_{IN2}$ $P0_1/S_{OUT2}$ $P0_2/S_{CLK2}$ $P0_3/\overline{S_{RDY2}}$	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •$P1_0$ to $P1_7$ (8 bits) are enabled to output large current for LED drive.	• Serial I/O2 function pin
$P0_4$–$P0_7$			
$P1_0$–$P1_7$	I/O port P1		
$P2_0/X_{COUT}$ $P2_1/X_{CIN}$	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •$P2_0$, $P2_1$, $P2_4$ to $P2_7$: CMOS3-state output structure. •$P2_2$, $P2_3$: N-channel open-drain structure.	• Sub-clock generating circuit I/O pins (connect a resonator)
$P2_2$ $P2_3$			
$P2_4/RxD$ $P2_5/TxD$			• Serial I/O1 function pin
$P2_6/S_{CLK}$			
$P2_7/CNTR_0/\overline{S_{RDY1}}$			• Serial I/O1 function pin/ Timer X function pin
$P3_0/AN_0$– $P3_4/AN_4$	I/O port P3	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• A-D converter input pin
$P4_0/CNTR_1$	I/O port P4	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• Timer Y function pin
$P4_1/INT_0$ $P4_2/INT_1$			• Interrupt input pins
$P4_3/INT_2/S_{CMP2}$			• Interrupt input pin • S_{CMP2} output pin
$P4_4/INT_3/PWM$			• Interrupt input pin • PWM output pin

PART NUMBERING

Product name M3850 3 M 4 H– XXX SP

Package type
SP : 42P4B
FP : 42P2R-A/E
SS : 42S1B-A

ROM number
Omitted in One Time PROM version shipped in blank,
EPROM version, and flash memory version.

– : standard
Omitted in One Time PROM version shipped in blank, EPROM version, and flash memory version.
H–: Partial specification changed version

ROM/PROM/Flash memory size

1 : 4096 bytes	9 : 36864 bytes
2 : 8192 bytes	A : 40960 bytes
3 : 12288 bytes	B : 45056 bytes
4 : 16384 bytes	C : 49152 bytes
5 : 20480 bytes	D : 53248 bytes
6 : 24576 bytes	E : 57344 bytes
7 : 28672 bytes	F : 61440 bytes
8 : 32768 bytes	

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used as a user's ROM area.
However, they can be programmed or erased in the flash memory version, so that the users can use them.

Memory type
M : Mask ROM version
E : EPROM or One Time PROM version
F : Flash memory version

RAM size

0 : 192 bytes	5 : 768 bytes
1 : 256 bytes	6 : 896 bytes
2 : 384 bytes	7 : 1024 bytes
3 : 512 bytes	8 : 1536 bytes
4 : 640 bytes	9 : 2048 bytes

Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 3850 group (spec. H) as follows.

Memory Type

Support for mask ROM, One Time PROM, and flash memory versions.

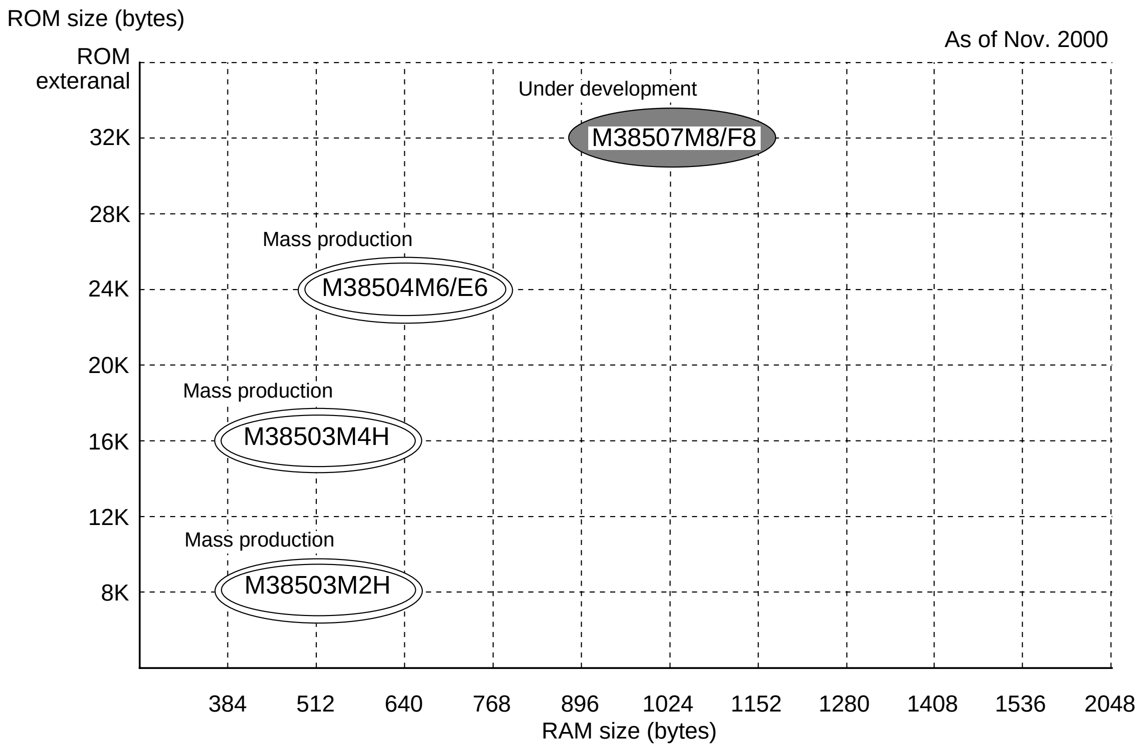
Memory Size

Flash memory size .... 32 K bytes
One Time PROM size .... 24 K bytes
Mask ROM size .... 8 K to 32 K bytes
RAM size .... 512 to 1 K bytes

Packages

42P4B .... 42-pin shrink plastic-molded DIP
42P2R-A/E .... 42-pin plastic-molded SOP
42S1B-A .... 42-pin shrink ceramic DIP (EPROM version)

Memory Expansion Plan



Products under development or planning: the development schedule and specification may be revised without notice.
The development of planning products may be stopped.

Fig. 4 Memory expansion plan

Currently planning products are listed below.

Table 2 Support products **As of Nov. 2000**

Product name	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38503M2H-XXXSP	8192 (8062)	512	42P4B	Mask ROM version
M38503M2H-XXXFP			42P2R-A/E	Mask ROM version
M38503M4H-XXXSP	16384 (16254)	512	424P4B	Mask ROM version
M38503M4H-XXXFP			42P2R-A/E	Mask ROM version
M38504M6-XXXSP	24576 (24446)	640	424P4B	Mask ROM version
M38504E6-XXXSP				One Time PROM version
M388504E6SP				One Time PROM version (blank)
M388504E6SS			42S1B-A	EPROM version
M38504M6-XXXFP			42P2R-A/E	Mask ROM version
M38504E6-XXXFP				One Time PROM version
M38504E6FP				One Time PROM version (blank)

Table 3 3850 group (standard) and 3850 group (spec. H) corresponding products

3850 group (standard)	3850 group (spec. H)
M38503M2-XXXFP/SP	M38503M2H-XXXFP/SP
M38503M4-XXXFP/SP	M38503M4H-XXXFP/SP
M38503E4-XXXFP/SP	M38504M6-XXXFP/SP
M38503E4FP/SP	M38504E6-XXXFP/SP
M38503E4SS	M38504E6FP/SP
	M38504E6SS
	M38507M8-XXXFP/SP
	M38507F8FP/SP
	M37516RSS

Table 4 Differences between 3850 group (standard) and 3850 group (spec. H)

	3850 group (standard)	3850 group (spec. H)
Serial I/O	1: Serial I/O (UART or Clock-synchronized)	2: Serial I/O1 (UART or Clock-synchronized) Serial I/O2 (Clock-synchronized)
A-D converter	Unserviceable in low-speed mode	Serviceable in low-speed mode
Large current port	5: $P1_3$–$P1_7$	8: $P1_0$–$P1_7$

Notes on differences between 3850 group (standard) and 3850 group (spec. H)

(1) The absolute maximum ratings of 3850 group (spec. H) is smaller than that of 3850 group (standard).
•Power source voltage Vcc = –0.3 to 6.5 V
•CNVss input voltage V_I = –0.3 to Vcc +0.3 V

(2) The oscillation circuit constants of X_{IN}-X_{OUT}, X_{CIN}-X_{COUT} may be some differences between 3850 group (standard) and 3850 group (spec. H).

(3) Do not write any data to the reserved area and the reserved bit. (Do not change the contents after rest.)

(4) Fix bit 3 of the CPU mode register to “1”.

(5) Be sure to perform the termination of unused pins.

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3850 group (spec. H) uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

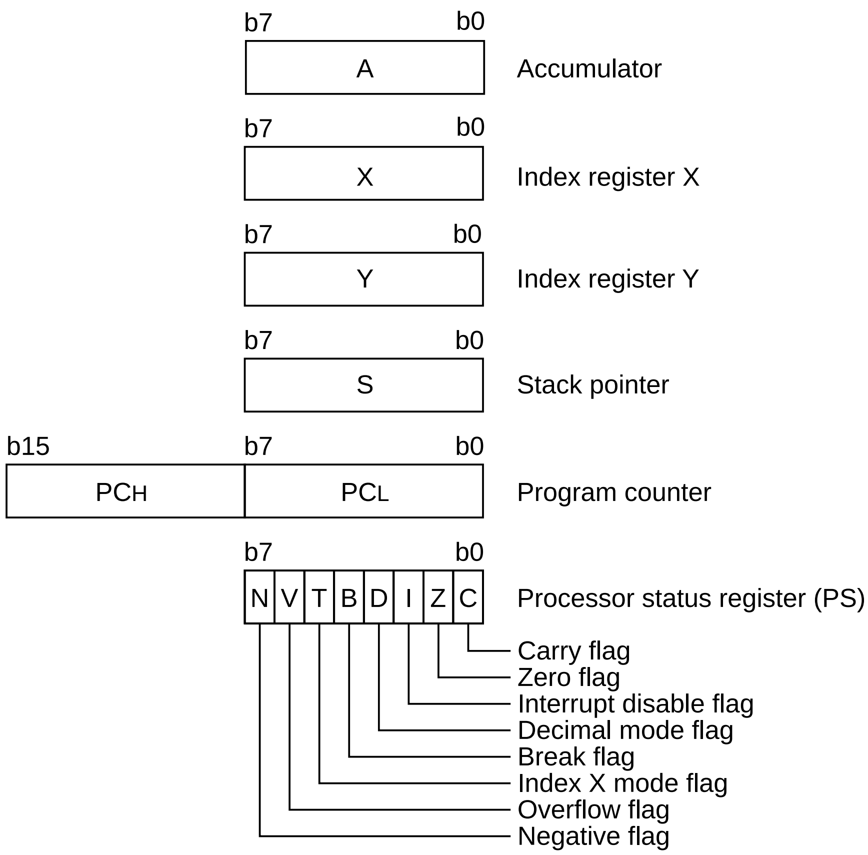


Fig. 5 740 Family CPU register structure

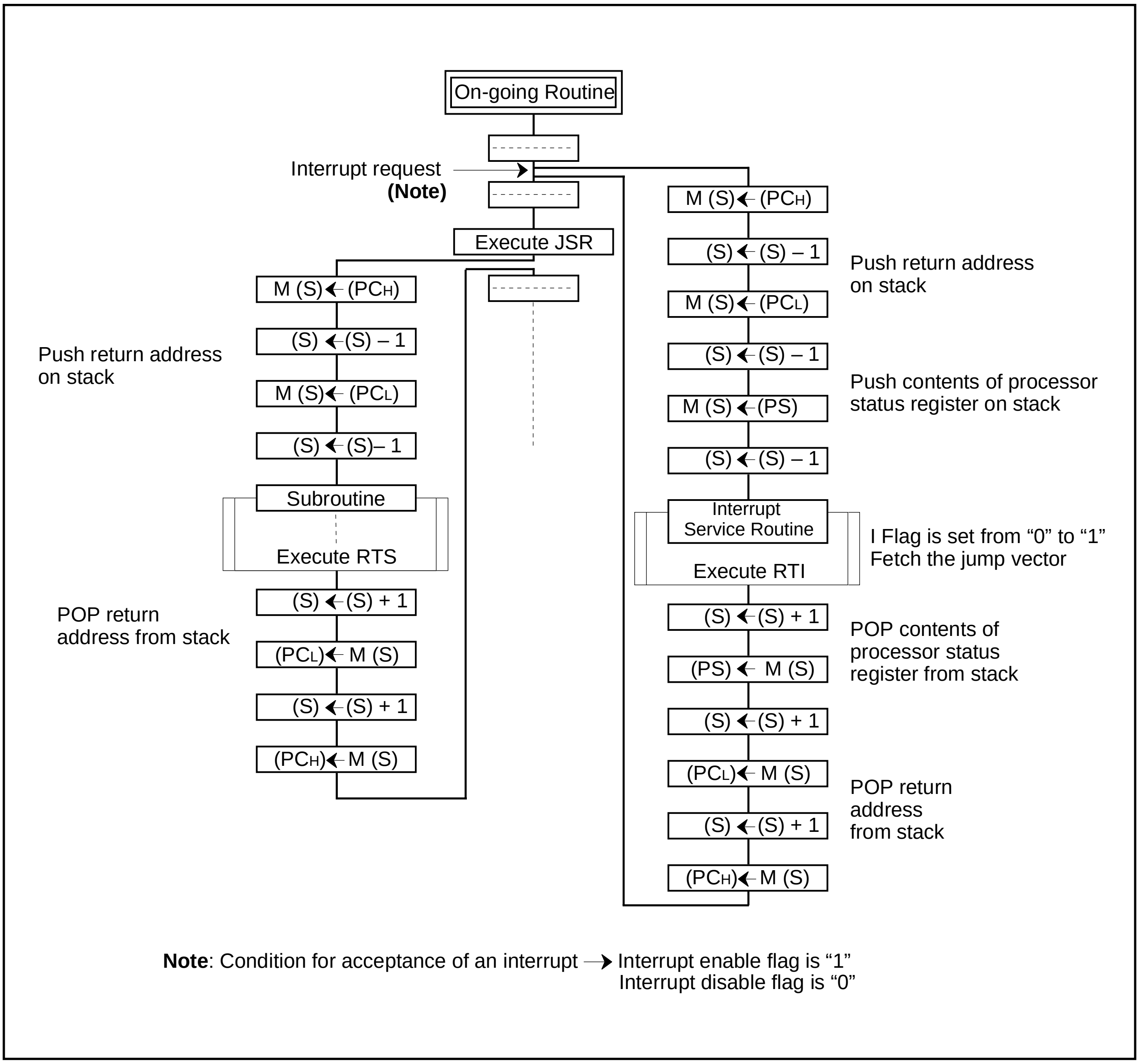


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 5 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)
When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 6 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] $003B_{16}$

The CPU mode register contains the stack page selection bit, etc.
The CPU mode register is allocated at address $003B_{16}$.

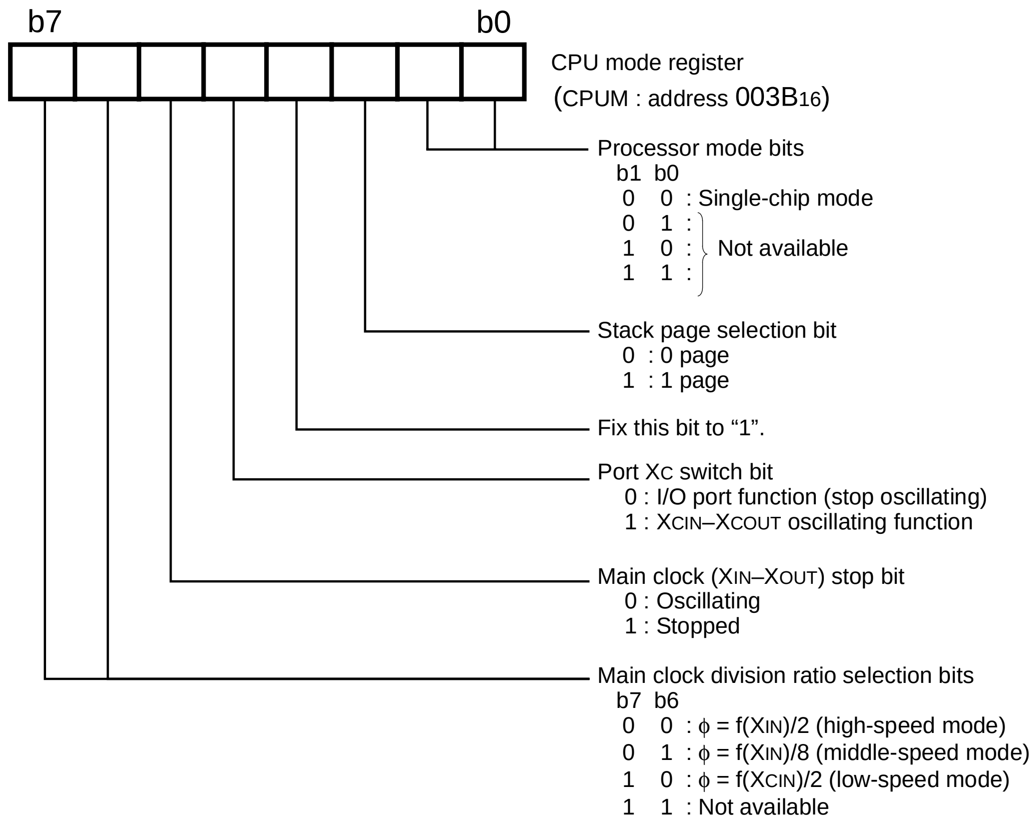


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

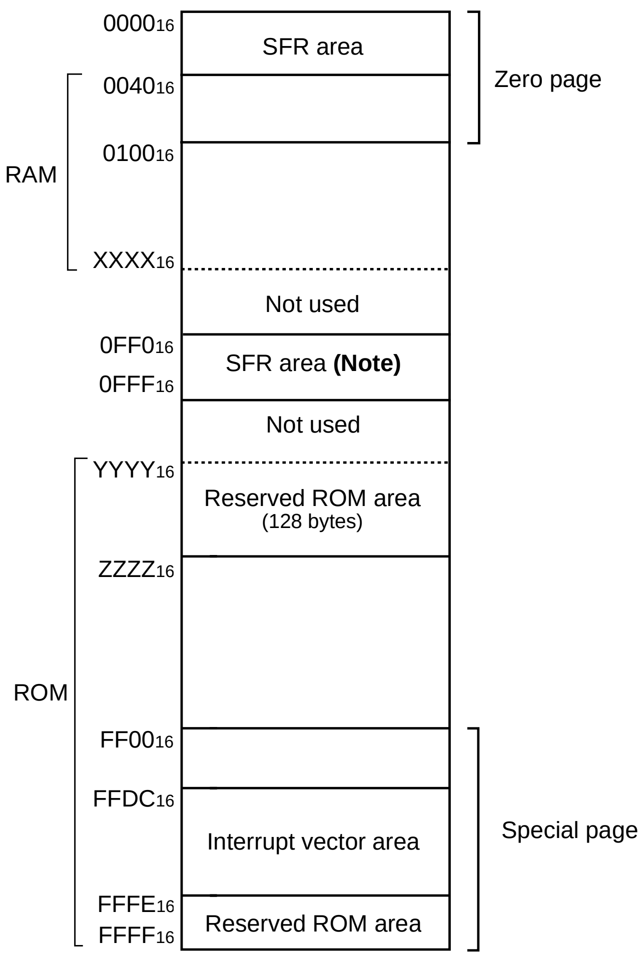
Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}



Note: Flash memory version only

Fig. 8 Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Prescaler 12 (PRE12)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer 1 (T1)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 2 (T2)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer XY mode register (TM)
0004_{16}	Port P2 (P2)	0024_{16}	Prescaler X (PREX)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer X (TX)
0006_{16}	Port P3 (P3)	0026_{16}	Prescaler Y (PREY)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer Y (TY)
0008_{16}	Port P4 (P4)	0028_{16}	Timer count source selection register (TCSS)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	
$000A_{16}$		$002A_{16}$	
$000B_{16}$		$002B_{16}$	Reserved ✻
$000C_{16}$		$002C_{16}$	Reserved ✻
$000D_{16}$		$002D_{16}$	Reserved ✻
$000E_{16}$		$002E_{16}$	Reserved ✻
$000F_{16}$		$002F_{16}$	Reserved ✻
0010_{16}		0030_{16}	Reserved ✻
0011_{16}		0031_{16}	Reserved ✻
0012_{16}	Reserved ✻	0032_{16}	
0013_{16}	Reserved ✻	0033_{16}	
0014_{16}	Reserved ✻	0034_{16}	A-D control register (ADCON)
0015_{16}	Serial I/O2 control register 1 (SIO2CON1)	0035_{16}	A-D conversion low-order register (ADL)
0016_{16}	Serial I/O2 control register 2 (SIO2CON2)	0036_{16}	A-D conversion high-order register (ADH)
0017_{16}	Serial I/O2 register (SIO2)	0037_{16}	Reserved ✻
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIOSTS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIOCON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	PWM control register (PWMCON)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	PWM prescaler (PREPWM)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	PWM register (PWM)	$003F_{16}$	Interrupt control register 2 (ICON2)

✻ Reserved : Do not write any data to this addresses, because these areas are reserved.

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Table 7 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P0$_0$/S$_{IN2}$ P0$_1$/S$_{OUT2}$ P0$_2$/S$_{CLK2}$ P0$_3$/$\overline{S_{RDY2}}$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1) (2) (3) (4)
P0$_4$–P0$_7$						(5)
P1$_0$–P1$_7$	Port P1					
P2$_0$/X$_{COUT}$ P2$_1$/X$_{CIN}$	Port P2			Sub-clock generating circuit	CPU mode register	(6) (7)
P2$_2$ P2$_3$			CMOS compatible input level N-channel open-drain output			(8)
P2$_4$/RxD P2$_5$/TxD P2$_6$/S$_{CLK}$			CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O	Serial I/O1 control register	(9) (10) (11)
P2$_7$/CNTR$_0$/$\overline{S_{RDY1}}$				Serial I/O1 function I/O Timer X function I/O	Serial I/O1 control register Timer XY mode register	(12)
P3$_0$/AN$_0$– P3$_4$/AN$_4$	Port P3			A-D conversion input	A-D control register	(13)
P4$_0$/CNTR$_1$	Port P4			Timer Y function I/O	Timer XY mode register	(14)
P4$_1$/INT$_0$ P4$_2$/INT$_1$				External interrupt input	Interrupt edge selection register	(15)
P4$_3$/INT$_2$/S$_{CMP2}$				External interrupt input S$_{CMP2}$ output	Interrupt edge selection register Serial I/O2 control register	(16)
P4$_4$/INT$_3$/PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(17)

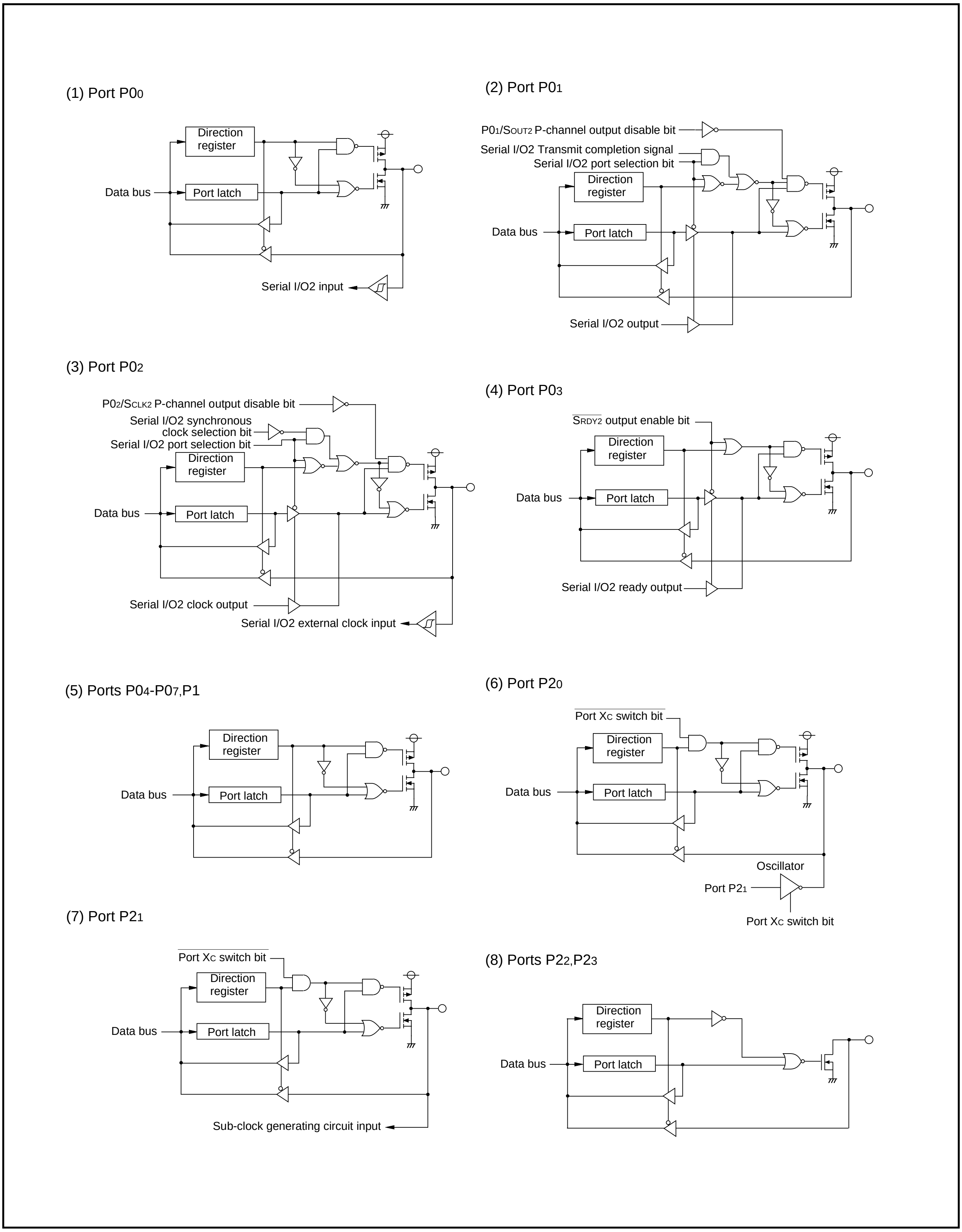


Fig. 10 Port block diagram (1)

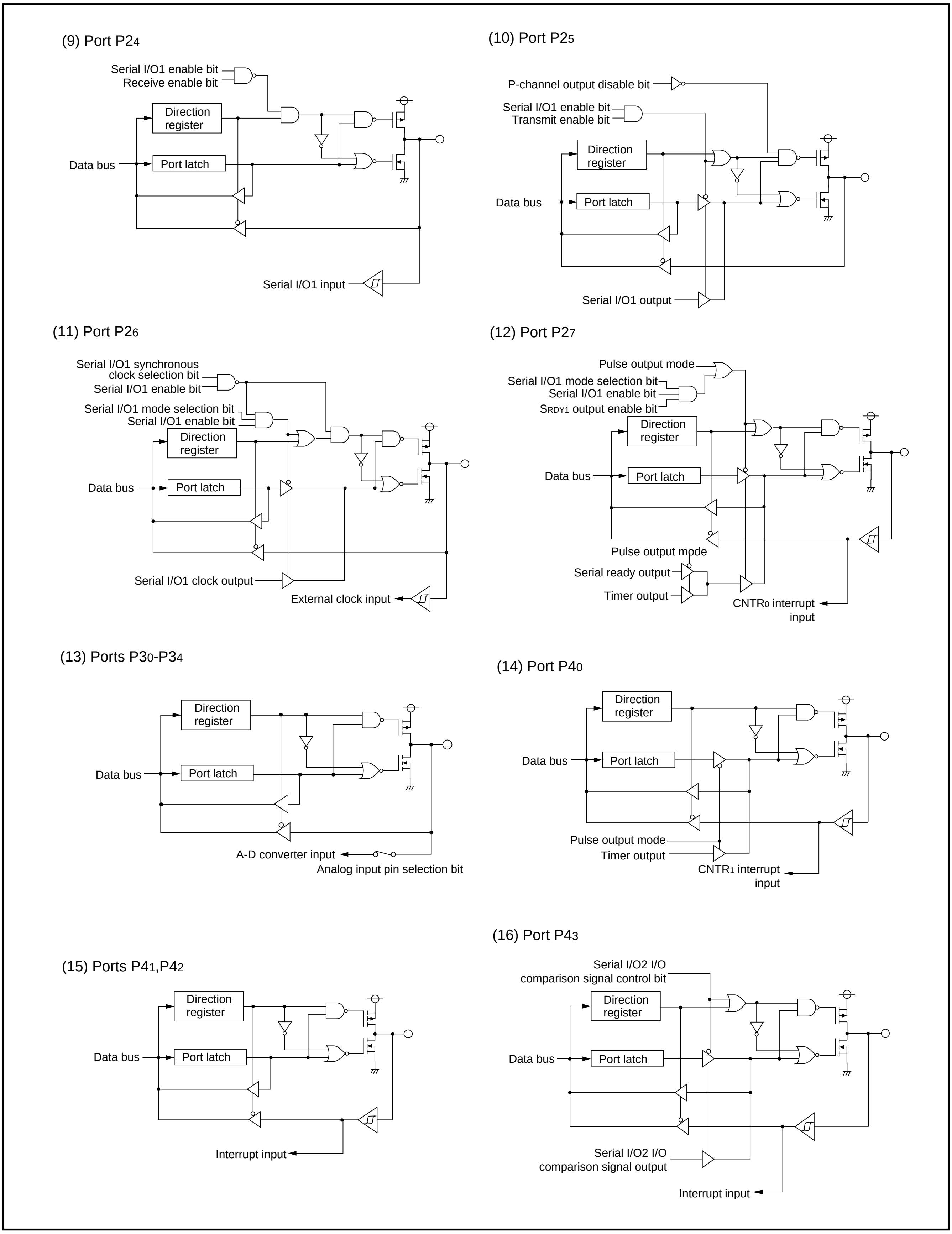


Fig. 11 Port block diagram (2)

(17) Port $P4_4$

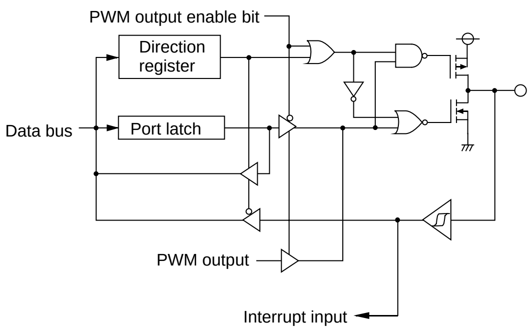


Fig. 12 Port block diagram (3)

INTERRUPTS

Interrupts occur by 15 sources among 15 sources: six external, eight internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.
Interrupt enable bits can be set or cleared by software.
Interrupt request bits can be cleared by software, but cannot be set by software.
The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.
When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes

When the active edge of an external interrupt (INT_0–INT_3, $CNTR_0$, $CNTR_1$) is set, the corresponding interrupt request bit may also be set. Therefore, take the following sequence:

1. Disable the interrupt
2. Change the interrupt edge selection register (the timer XY mode register for $CNTR_0$ and $CNTR_1$)
3. Clear the interrupt request bit to “0”
4. Accept the interrupt.

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
Reserved	3	$FFF9_{16}$	$FFF8_{16}$	Reserved	
INT_1	4	$FFF7_{16}$	$FFF6_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
INT_2	5	$FFF5_{16}$	$FFF4_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3/ Serial I/O2	6	$FFF3_{16}$	$FFF2_{16}$	At detection of either rising or falling edge of INT_3 input/ At completion of serial I/O2 data reception/transmission	External interrupt (active edge selectable) Switch by Serial I/O2/INT_3 interrupt source bit
Reserved	7	$FFF1_{16}$	$FFF0_{16}$	Reserved	
Timer X	8	$FFEF_{16}$	$FFEE_{16}$	At timer X underflow	
Timer Y	9	$FFED_{16}$	$FFEC_{16}$	At timer Y underflow	
Timer 1	10	$FFEB_{16}$	$FFEA_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	11	$FFE9_{16}$	$FFE8_{16}$	At timer 2 underflow	
Serial I/O1 reception	12	$FFE7_{16}$	$FFE6_{16}$	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	13	$FFE5_{16}$	$FFE4_{16}$	At completion of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
$CNTR_0$	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	15	$FFE1_{16}$	$FFE0_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
A-D converter	16	$FFDF_{16}$	$FFDE_{16}$	At completion of A-D conversion	
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

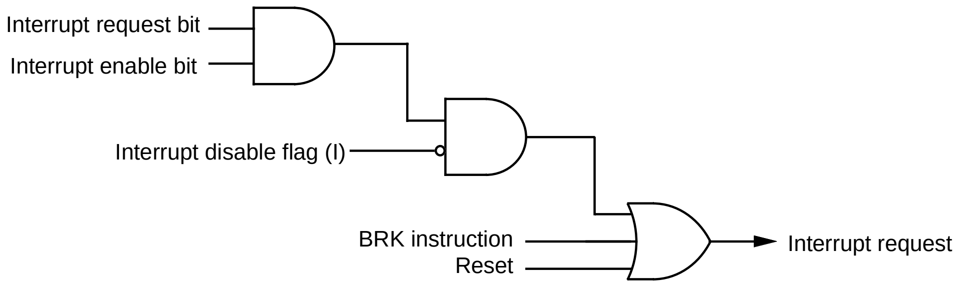


Fig. 13 Interrupt control

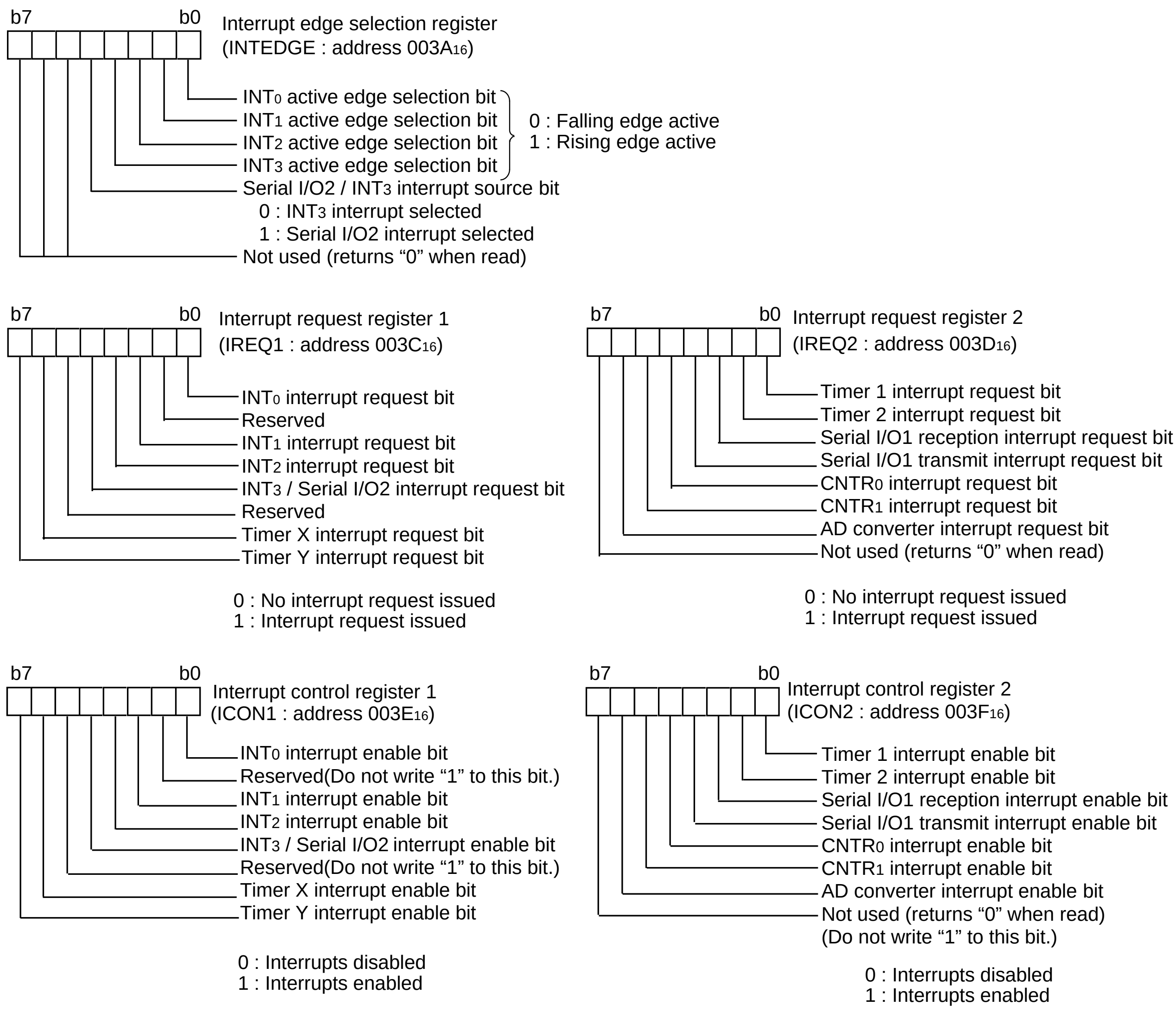


Fig. 14 Structure of interrupt-related registers

TIMERS

The 3850 group (spec. H) has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are count down. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

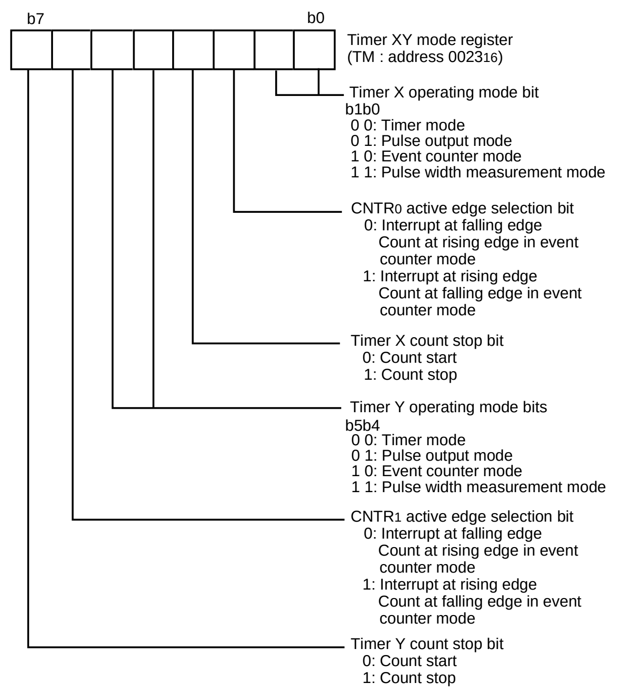


Fig. 15 Structure of timer XY mode register

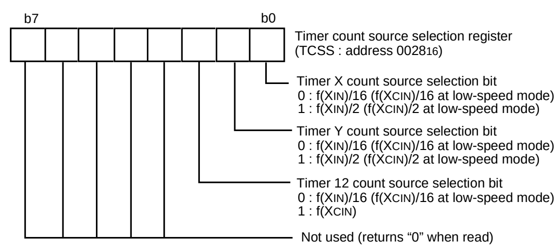


Fig. 16 Structure of timer count source selection register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency which is selected by timer 12 count source selection bit. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select in one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts the count source selected by Timer count source selection bit.

(2) Pulse Output Mode

The timer counts the count source selected by Timer count source selection bit. Whenever the contents of the timer reach "00_{16}", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", output begins at " H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P2_7$ (or port $P4_0$) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the rising edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the falling edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

(4) Pulse Width Measurement Mode

If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the timer counts the selected signals by the count source selection bit while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the timer counts it while the $CNTR_0$ (or $CNTR_1$) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.

■Note

When switching the count source by the timer 12, X and Y count source bit, the value of timer count is altered in unconsiderable amount owing to generating of a thin pulses in the count input signals.

Therefore, select the timer count source before set the value to the prescaler and the timer.

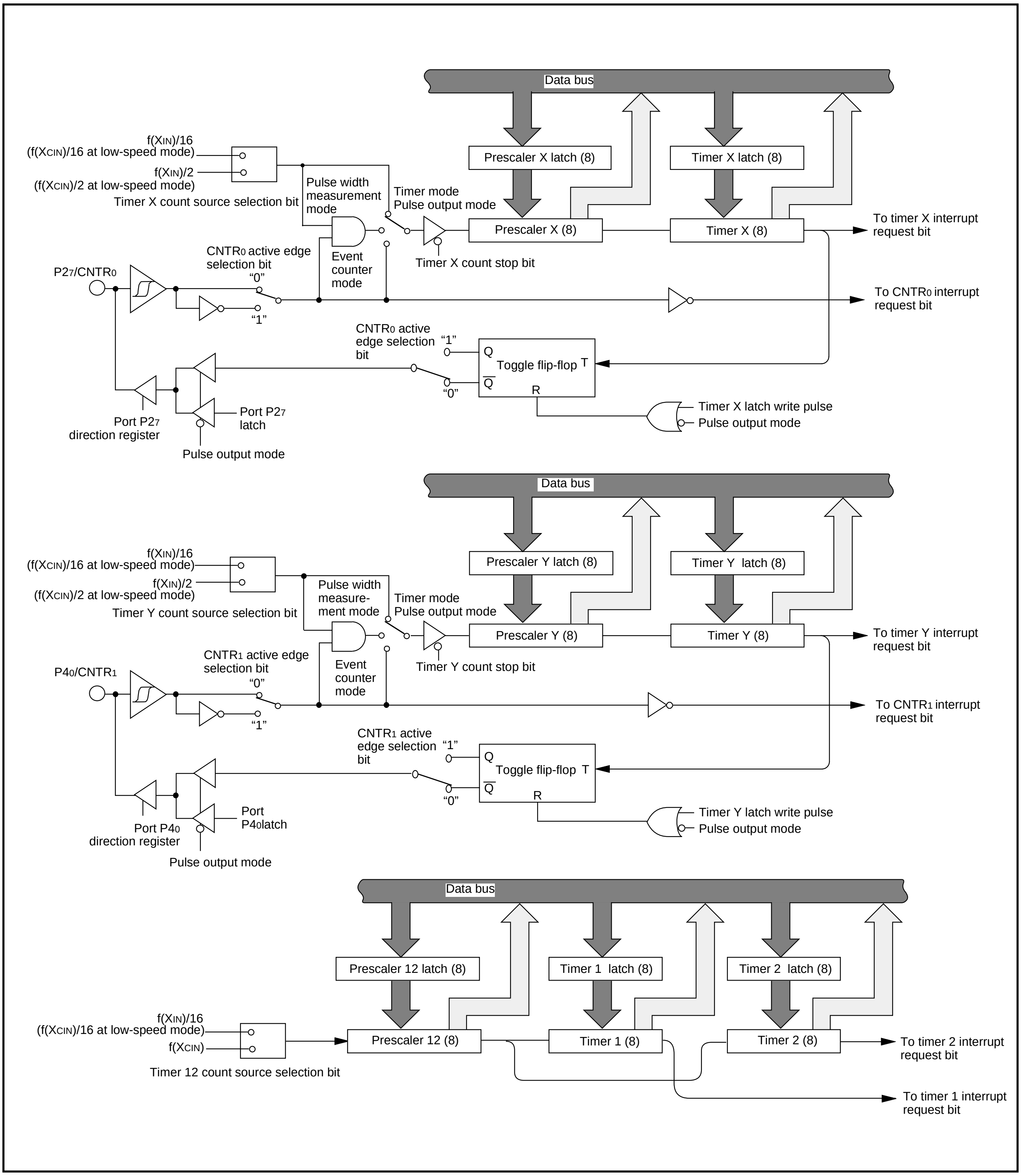


Fig. 17 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O

●SERIAL I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address $001A_{16}$) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

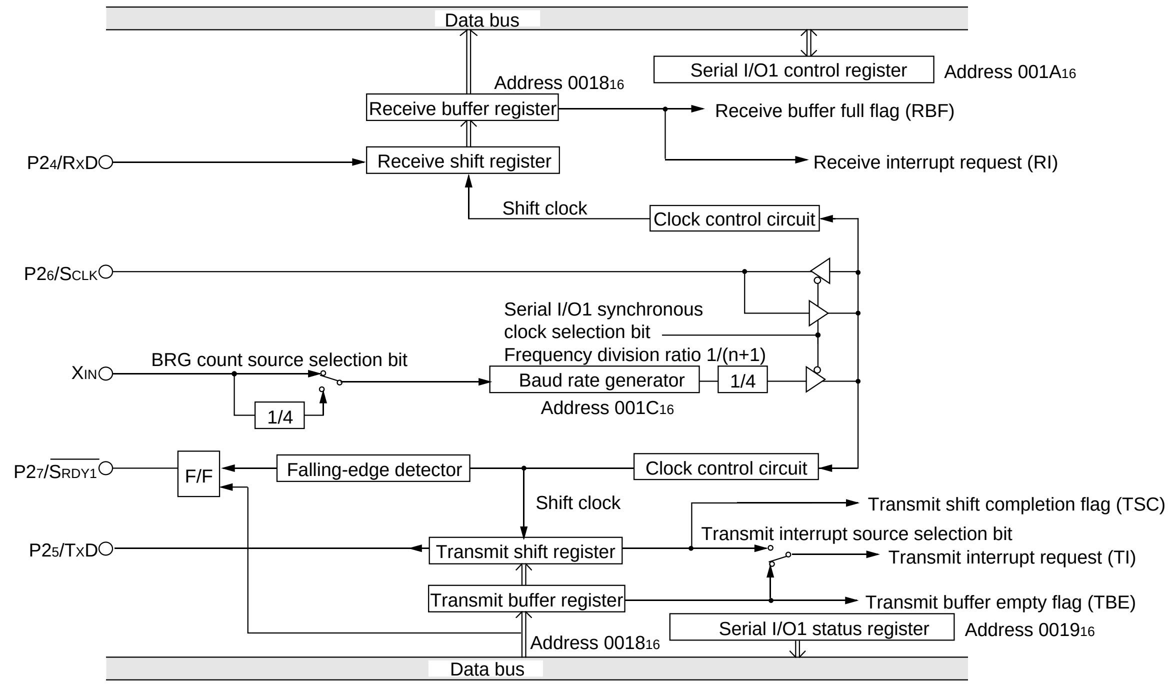
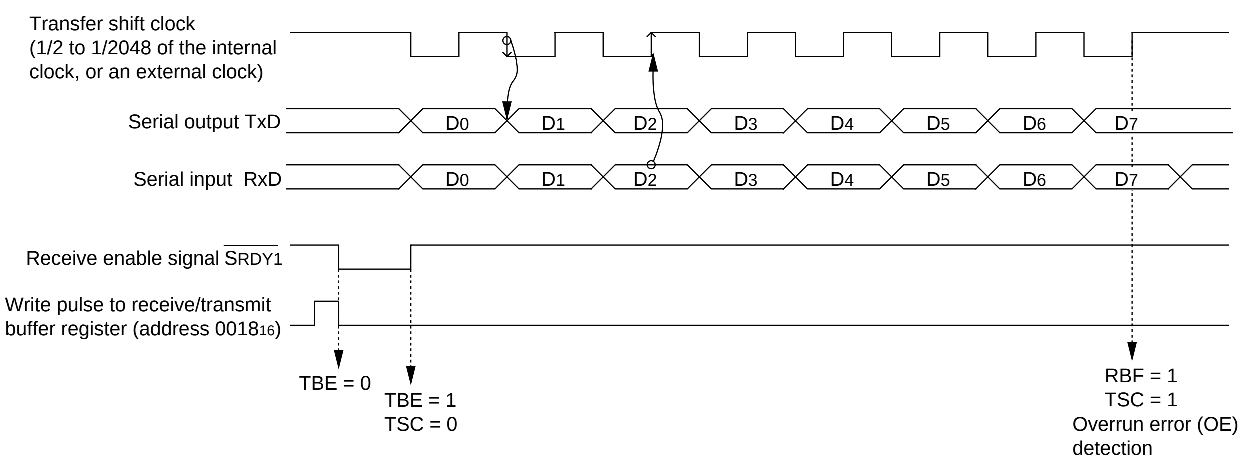


Fig. 18 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 19 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit (b6) of the serial I/O1 control register to “0”.
Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.
The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.
The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

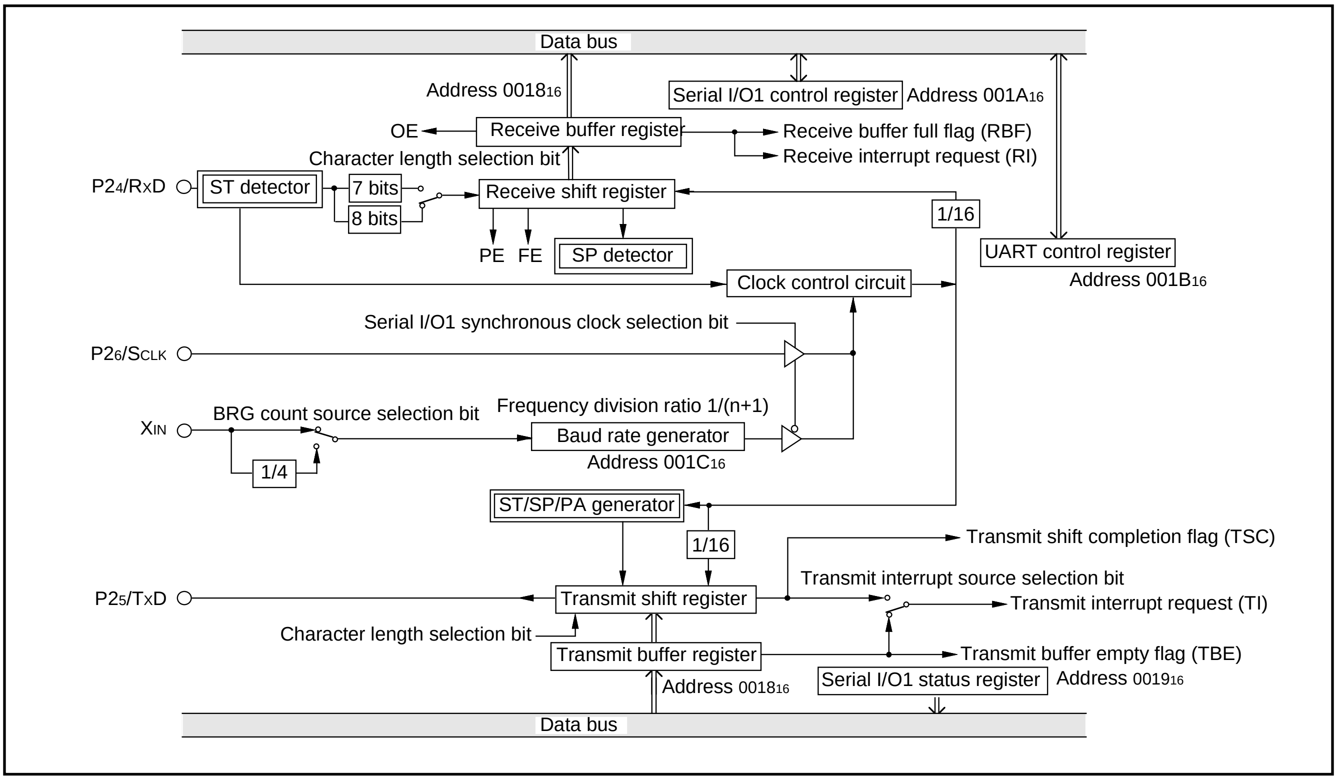
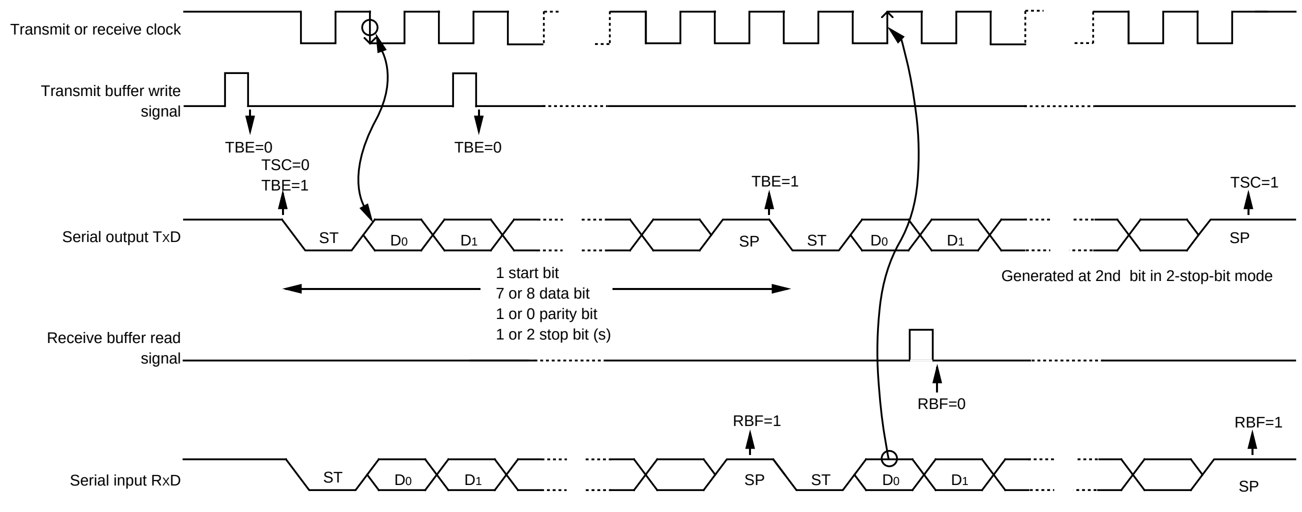


Fig. 20 Block diagram of UART serial I/O1



Notes **1:** Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1,” can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1.”
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 21 Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 0018_{16}

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Serial I/O1 Status Register (SIOSTS)] 0019_{16}

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.
Bits 0 to 6 of the serial I/O1 status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O1 Control Register (SIOCON)] $001A_{16}$

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] $001B_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the $P2_5$/TxD pin.

[Baud Rate Generator (BRG)] $001C_{16}$

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

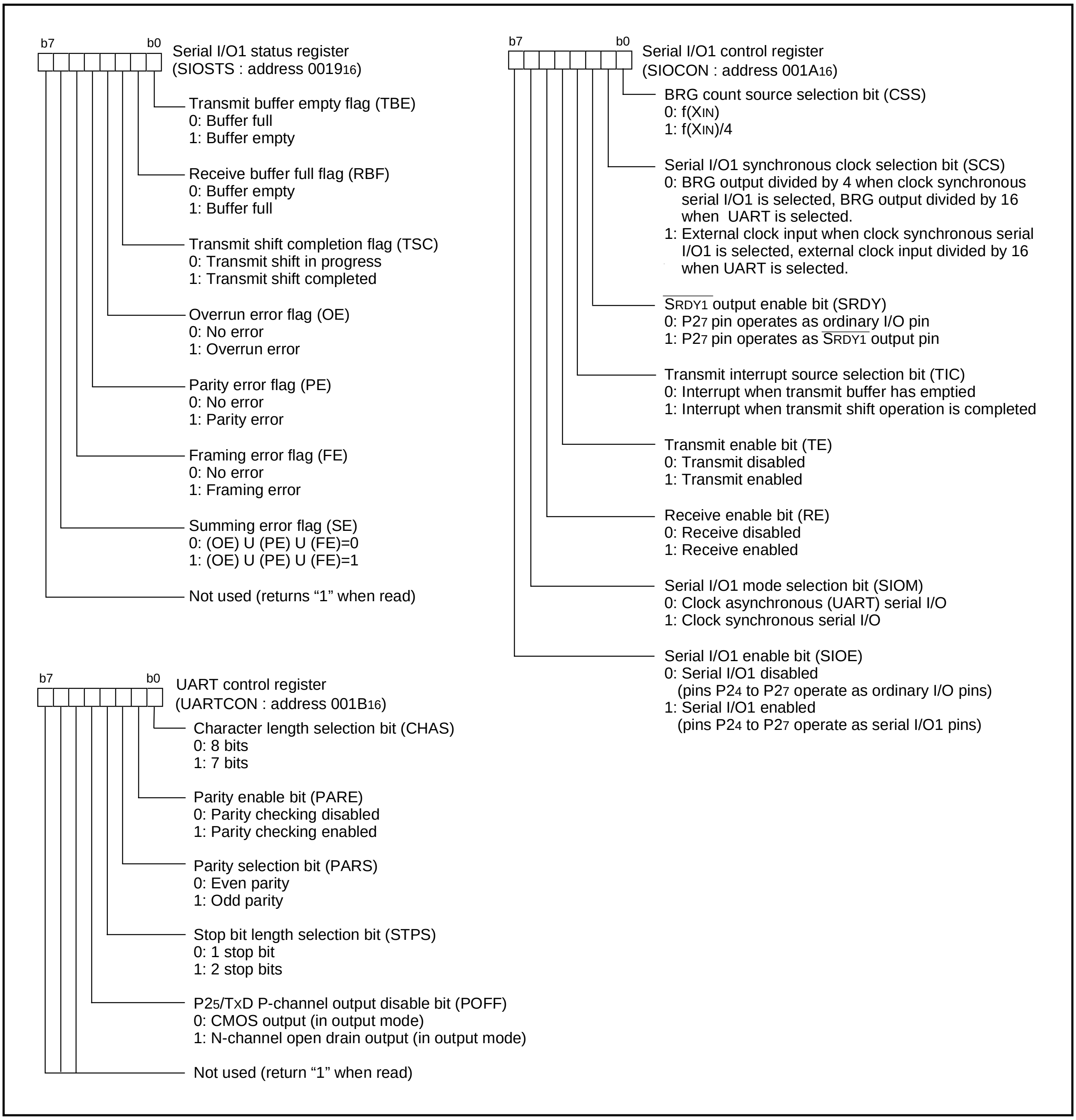


Fig. 22 Structure of serial I/O1 control registers

●SERIAL I/O2

The serial I/O2 can be operated only as the clock synchronous type. As a synchronous clock for serial transfer, either internal clock or external clock can be selected by the serial I/O2 synchronous clock selection bit (b6) of serial I/O2 control register 1.

The internal clock incorporates a dedicated divider and permits selecting 6 types of clock by the internal synchronous clock selection bits (b2, b1, b0) of serial I/O2 control register 1.

Regarding SOUT2 and SCLK2 being output pins, either CMOS output format or N-channel open-drain output format can be selected by the P01/SOUT2, P02/SCLK2 P-channel output disable bit (b7) of serial I/O2 control register 1.

When the internal clock has been selected, a transfer starts by a write signal to the serial I/O2 register (address 0017_{16}). After completion of data transfer, the level of the SOUT2 pin goes to high impedance automatically but bit 7 of the serial I/O2 control register 2 is not set to “1” automatically.

When the external clock has been selected, the contents of the serial I/O2 register is continuously sifted while transfer clocks are input. Accordingly, control the clock externally. Note that the SOUT2 pin does not go to high impedance after completion of data transfer.

To cause the SOUT2 pin to go to high impedance in the case where the external clock is selected, set bit 7 of the serial I/O2 control register 2 to “1” when SCLK2 is “H” after completion of data transfer. After the next data transfer is started (the transfer clock falls), bit 7 of the serial I/O2 control register 2 is set to “0” and the SOUT2 pin is put into the active state.

Regardless of the internal clock to external clock, the interrupt request bit is set after the number of bits (1 to 8 bits) selected by the optional transfer bit is transferred. In case of a fractional number of bits less than 8 bits as the last data, the received data to be stored in the serial I/O2 register becomes a fractional number of bits close to MSB if the transfer direction selection bit of serial I/O2 control register 1 is LSB first, or a fractional number of bits close to LSB if the said bit is MSB first. For the remaining bits, the previously received data is shifted.

At transmit operation using the clock synchronous serial I/O, the SCMP2 signal can be output by comparing the state of the transmit pin SOUT2 with the state of the receive pin SIN2 in synchronization with a rise of the transfer clock. If the output level of the SOUT2 pin is equal to the input level to the SIN2 pin, “L” is output from the SCMP2 pin. If not, “H” is output. At this time, an INT2 interrupt request can also be generated. Select a valid edge by bit 2 of the interrupt edge selection register (address $003A_{16}$).

[Serial I/O2 Control Registers 1, 2 (SIO2CON1 / SIO2CON2)] 0015_{16}, 0016_{16}

The serial I/O2 control registers 1 and 2 are containing various selection bits for serial I/O2 control as shown in Figure 23.

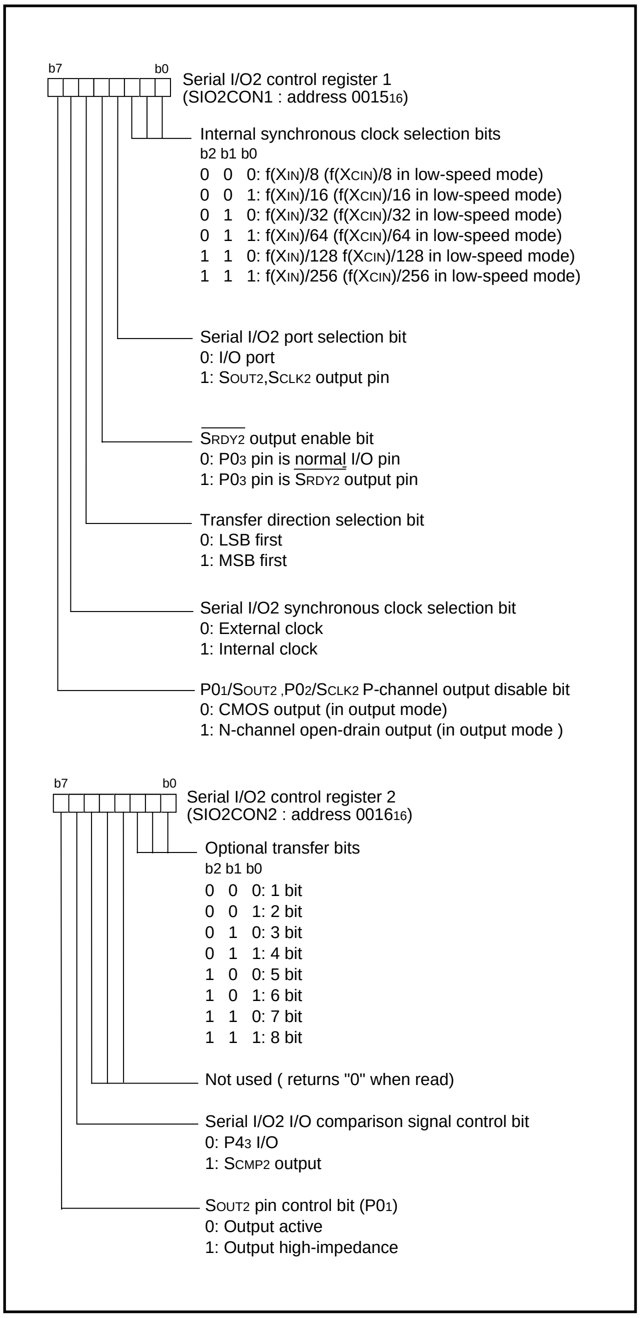


Fig. 23 Structure of Serial I/O2 control registers 1, 2

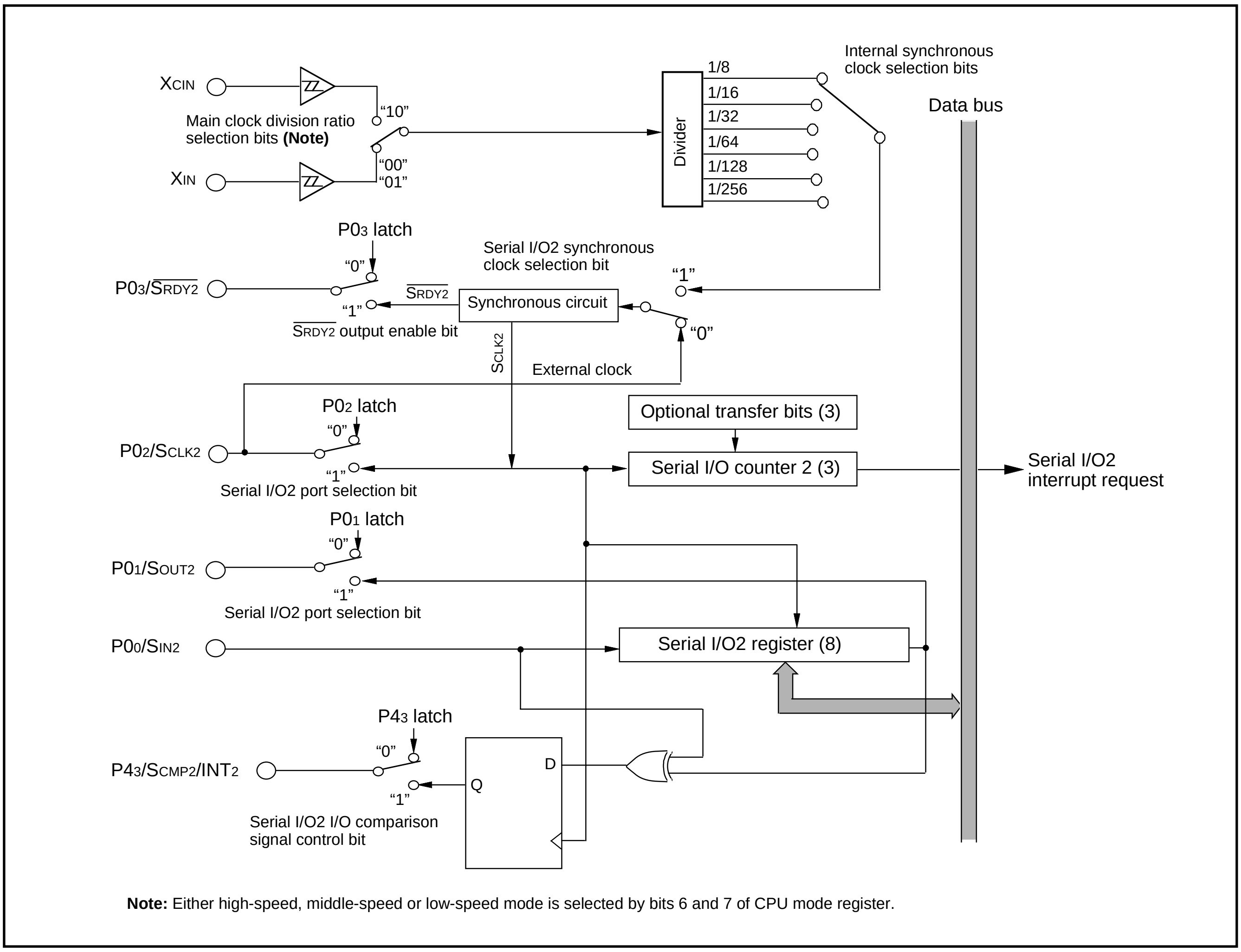


Fig. 24 Block diagram of Serial I/O2

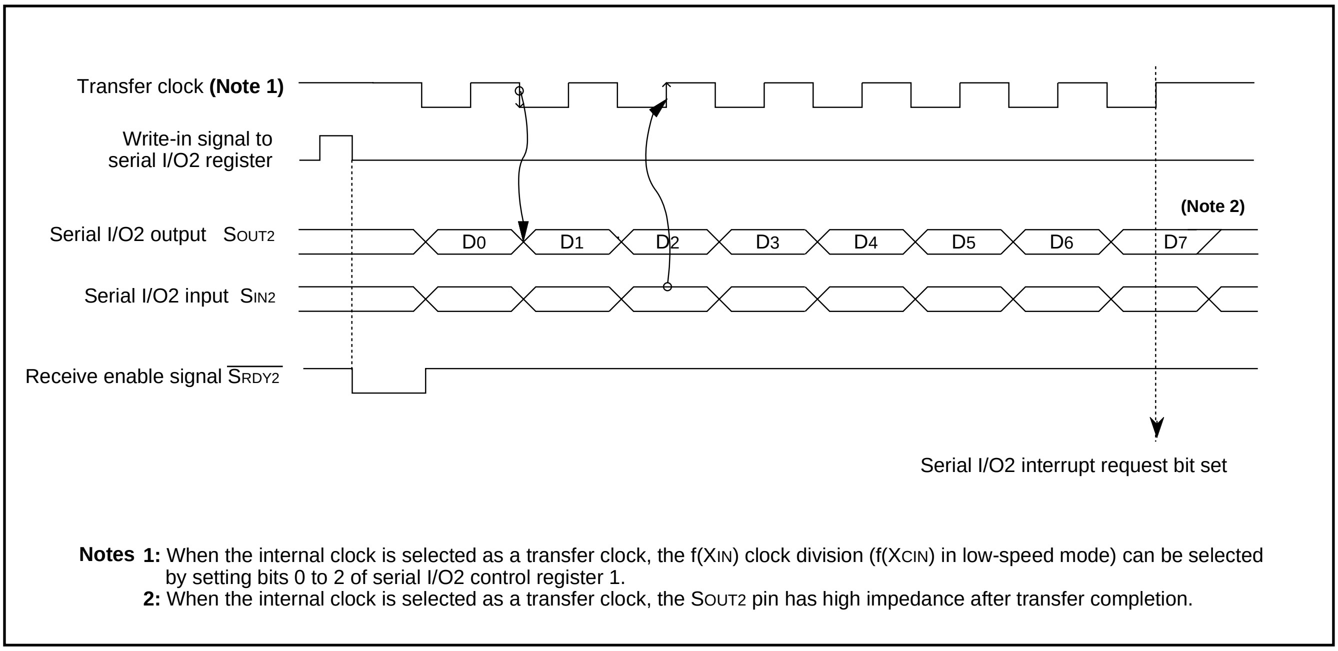


Fig. 25 Timing chart of Serial I/O2

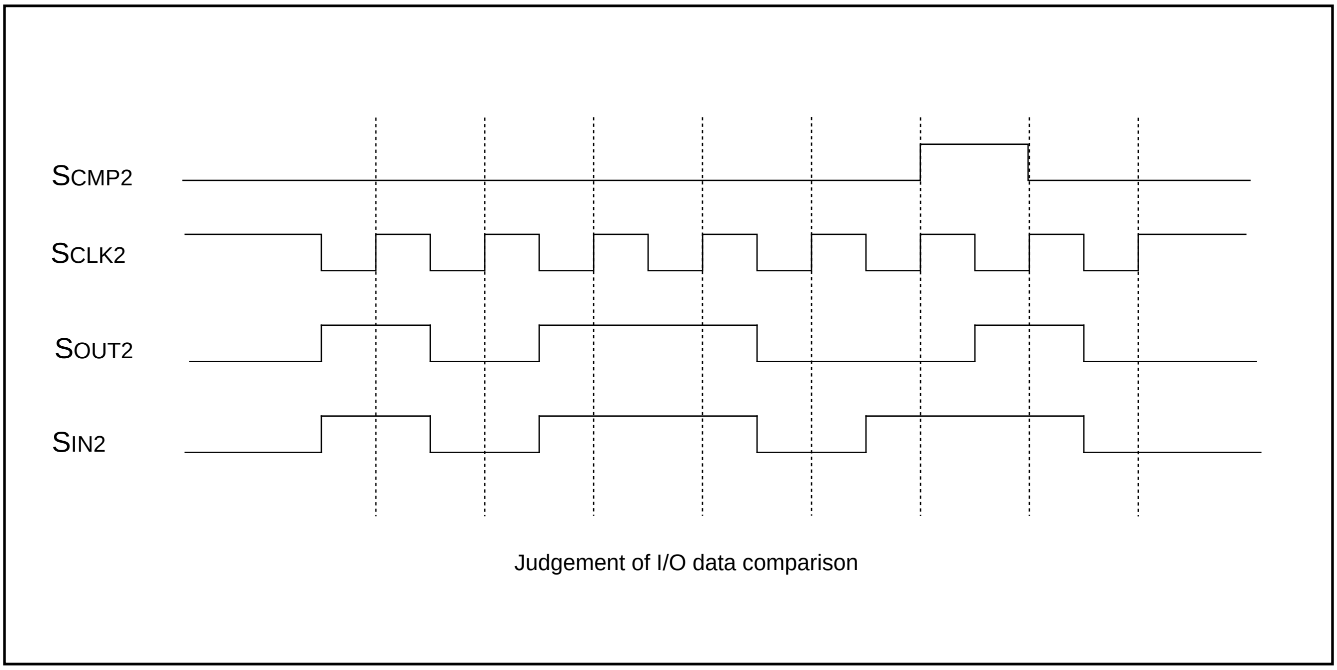


Fig. 26 SCMP2 output operation

PULSE WIDTH MODULATION (PWM)

The 3850 group (spec. H) has a PWM function with an 8-bit resolution, based on a signal that is the clock input X_{IN} or that clock input divided by 2.

Data Setting

The PWM output pin also functions as port $P4_4$. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

PWM period = 255 × (n+1) / f(X_{IN})
= 31.875 × (n+1) µs
(when f(X_{IN}) = 8 MHz,count source selection bit = "0")

Output pulse "H" term = PWM period × m / 255
= 0.125 × (n+1) × m µs
(when f(X_{IN}) = 8 MHz,count source selection bit = "0")

PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

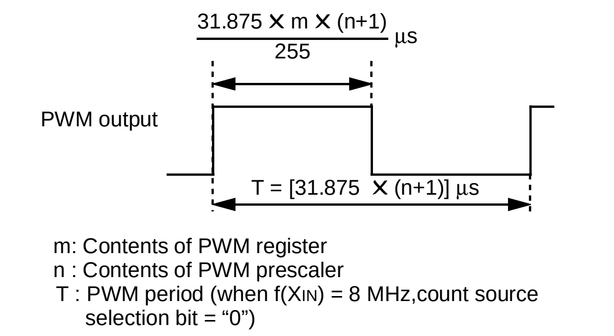


Fig. 27 Timing of PWM period

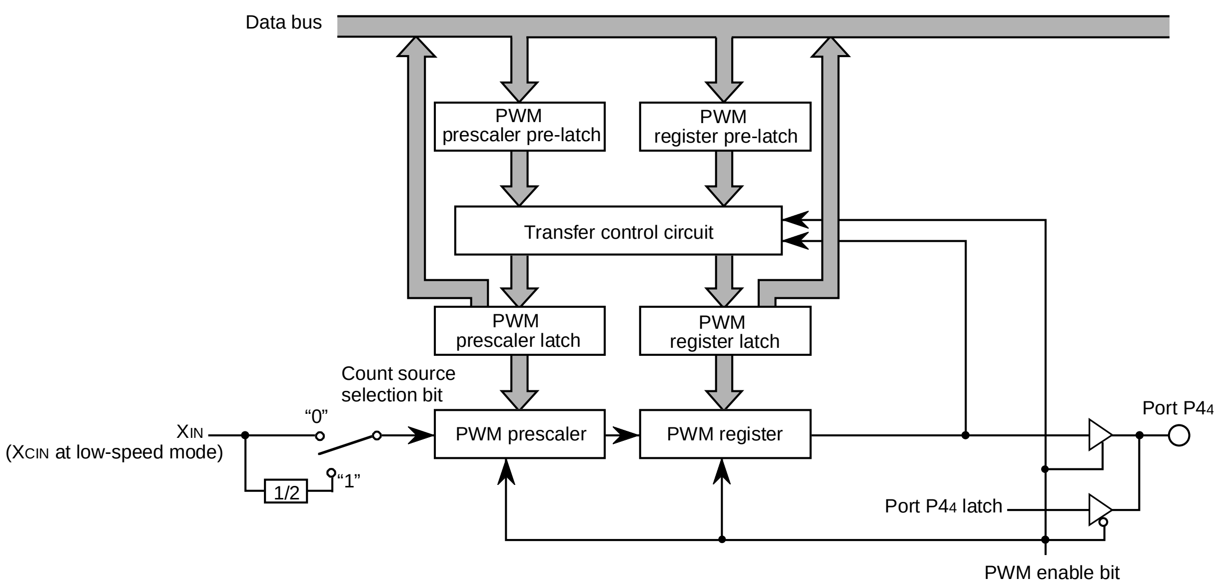


Fig. 28 Block diagram of PWM function

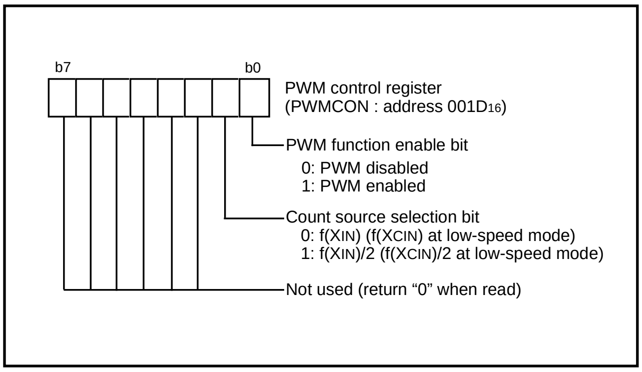


Fig. 29 Structure of PWM control register

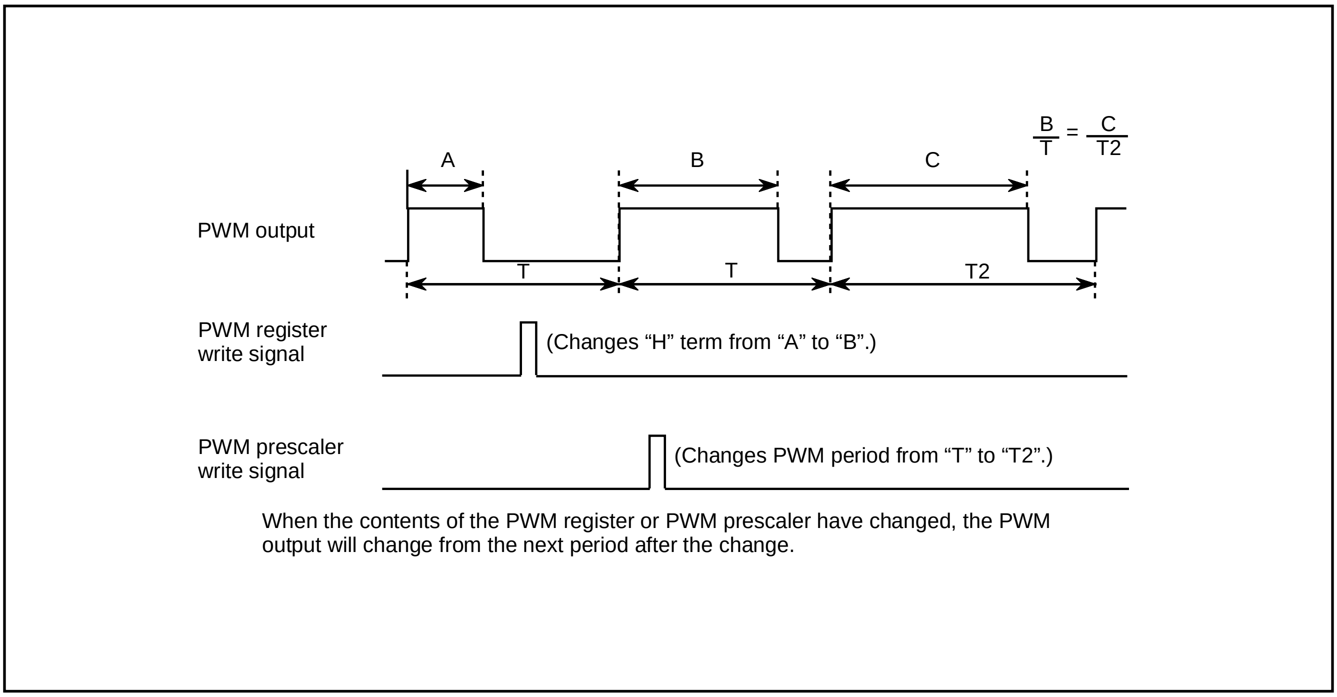


Fig. 30 PWM output timing when PWM register or PWM prescaler is changed

■Note

The PWM starts after the PWM function enable bit is set to enable and "L" level is output from the PWM pin.
The length of this "L" level output is as follows:

$\frac{n+1}{2 \cdot f(X_{IN})}$ sec (Count source selection bit = 0, where n is the value set in the prescaler)

$\frac{n+1}{f(X_{IN})}$ sec (Count source selection bit = 1, where n is the value set in the prescaler)

A-D CONVERTER

[A-D Conversion Registers (ADL, ADH)] 0035_{16}, 0036_{16}

The A-D conversion registers are read-only registers that store the result of an A-D conversion. Do not read these registers during an A-D conversion.

[AD Control Register (ADCON)] 0034_{16}

The AD control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 4 indicates the completion of an A-D conversion. The value of this bit remains at “0” during an A-D conversion and changes to “1” when an A-D conversion ends. Writing “0” to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} into 1024 and outputs the divided voltages.

Channel Selector

The channel selector selects one of ports $P3_0/AN_0$ to $P3_4/AN_4$ and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage, and the result is stored in the A-D conversion registers. When an A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to “1”.

Note that because the comparator consists of a capacitor coupling, set $f(X_{IN})$ to 500 kHz or more during an A-D conversion.

When the A-D converter is operated at low-speed mode, $f(X_{IN})$ and $f(X_{CIN})$ do not have the lower limit of frequency, because of the A-D converter has a built-in self-oscillation circuit.

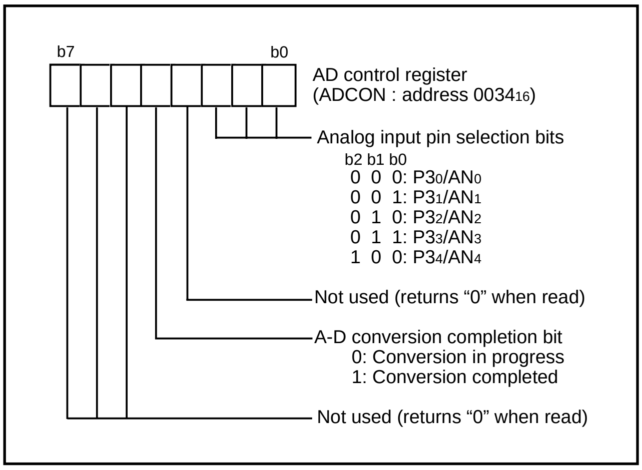


Fig. 31 Structure of AD control register

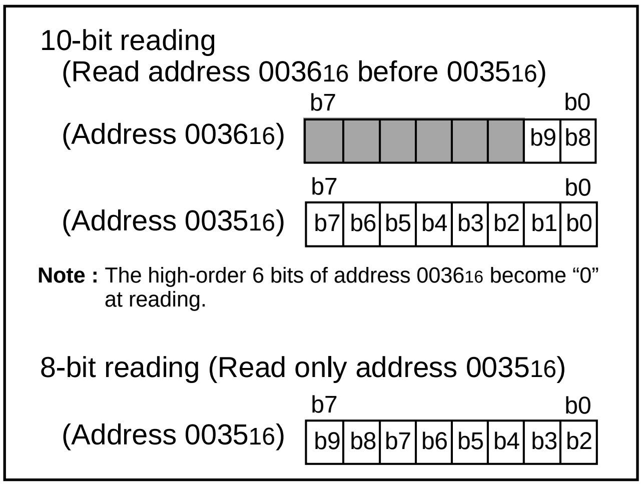


Fig. 32 Structure of A-D conversion registers

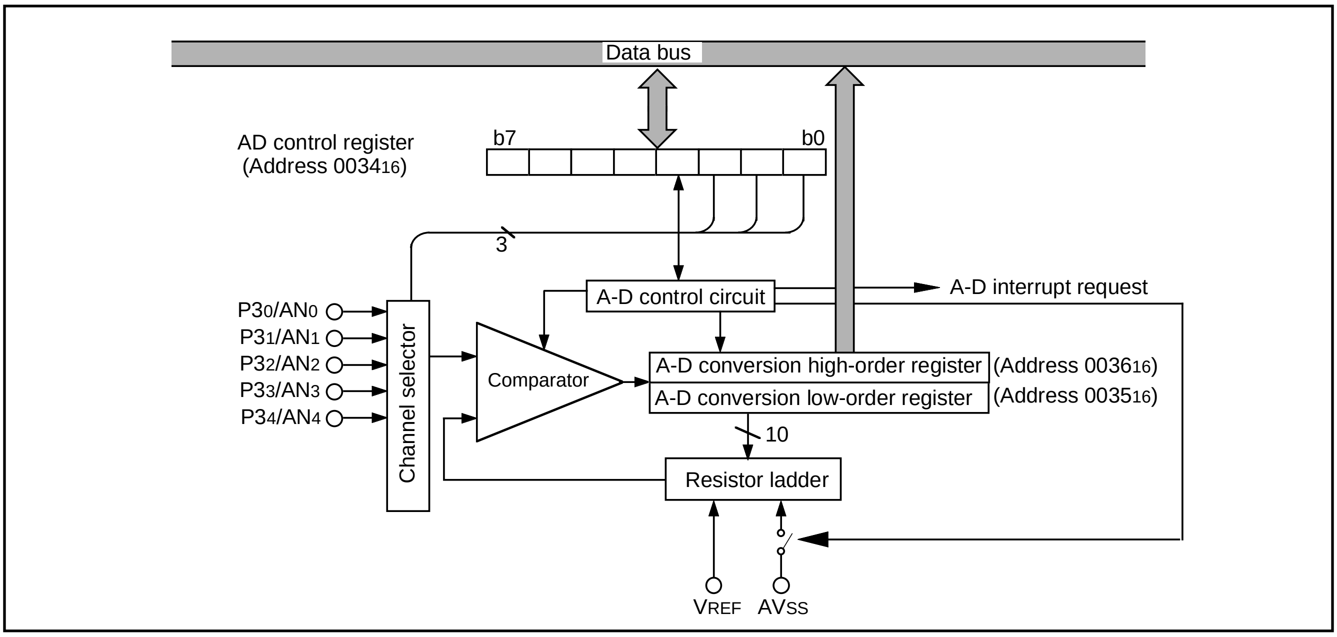


Fig. 33 Block diagram of A-D converter

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (address 0039_{16}) after reset, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 0039_{16}) and an internal reset occurs at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0039_{16}) may be started before an underflow. When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

●Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0039_{16}), each watchdog timer H and L is set to "FF_{16}."

●Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0039_{16}) permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to 131.072 ms at $f(X_{IN})$ = 8 MHz frequency and 32.768 s at $f(X_{CIN})$ = 32 kHz frequency.

When this bit is set to "1", the count source becomes the signal divided by 16 for $f(X_{IN})$ (or $f(X_{CIN})$). The detection time in this case is set to 512 µs at $f(X_{IN})$ = 8 MHz frequency and 128 ms at $f(X_{CIN})$ = 32 kHz frequency. This bit is cleared to "0" after reset.

●Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0039_{16}) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, once the STP instruction is executed, an internal reset occurs. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after reset.

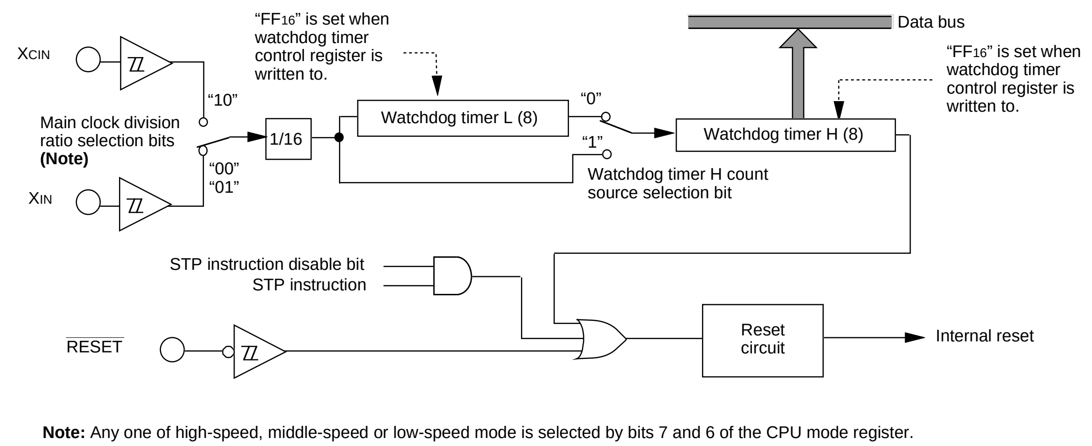


Fig. 34 Block diagram of Watchdog timer

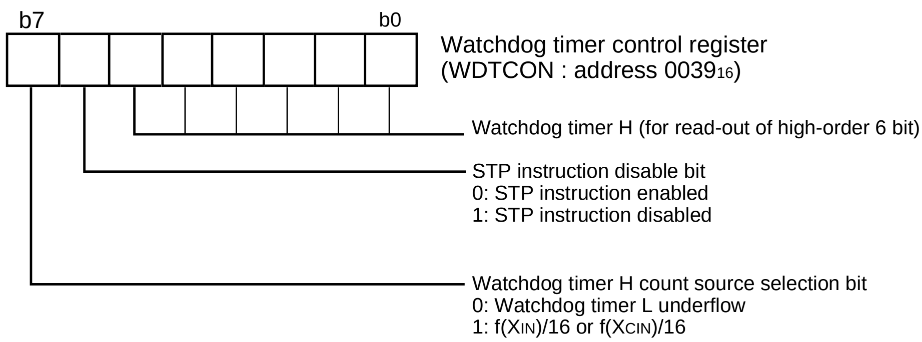


Fig. 35 Structure of Watchdog timer control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin must be held at an “L” level for 20 cycles or more of XIN. Then the $\overline{\text{RESET}}$ pin is returned to an “H” level (the power source voltage must be between 2.7 V and 5.5 V, and the oscillation must be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.54 V for VCC of 2.7 V.

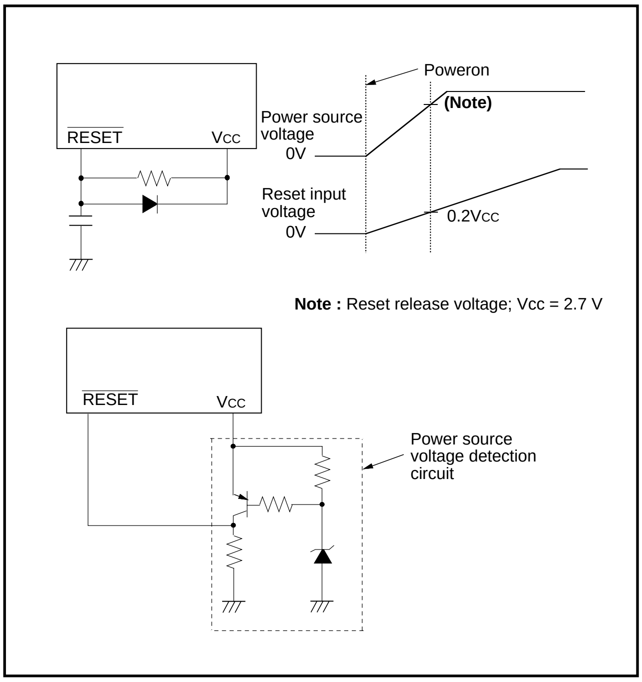


Fig. 36 Reset circuit example

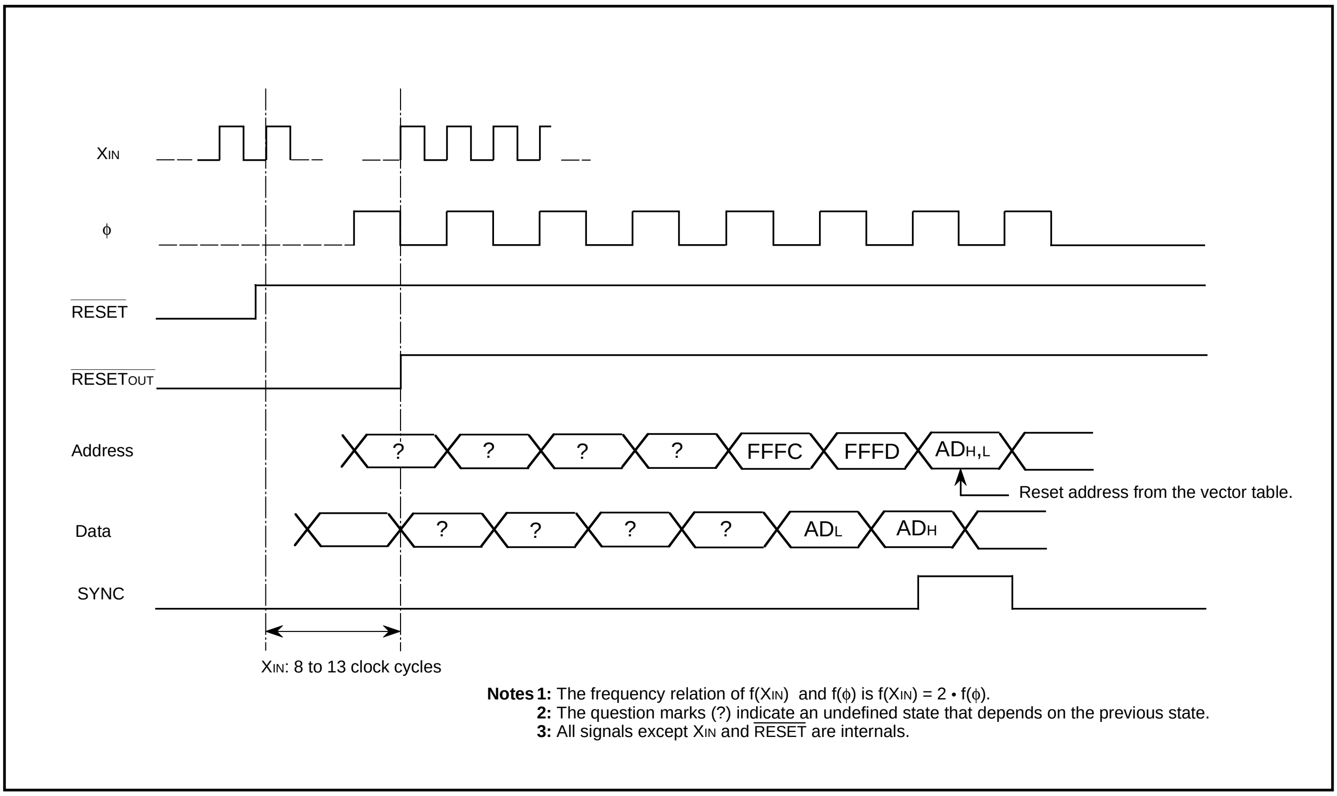


Fig. 37 Reset sequence

	Register	Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Serial I/O2 control register 1 (SIO2CON1)	0015_{16}	00_{16}
(12)	Serial I/O2 control register 2 (SIO2CON2)	0016_{16}	0 0 0 0 0 1 1 1
(13)	Serial I/O2 register (SIO2)	0017_{16}	X X X X X X X X
(14)	Transmit/Receive buffer register (TB/RB)	0018_{16}	X X X X X X X X
(15)	Serial I/O1 status register (SIOSTS)	0019_{16}	1 0 0 0 0 0 0 0
(16)	Serial I/O1 control register (SIOCON)	$001A_{16}$	00_{16}
(17)	UART control register (UARTCON)	$001B_{16}$	1 1 1 0 0 0 0 0
(18)	Baud rate generator (BRG)	$001C_{16}$	X X X X X X X X
(19)	PWM control register (PWMCON)	$001D_{16}$	00_{16}
(20)	PWM prescaler (PREPWM)	$001E_{16}$	X X X X X X X X
(21)	PWM register (PWM)	$001F_{16}$	X X X X X X X X
(22)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(23)	Timer 1 (T1)	0021_{16}	01_{16}
(24)	Timer 2 (T2)	0022_{16}	00_{16}
(25)	Timer XY mode register (TM)	0023_{16}	00_{16}
(26)	Prescaler X (PREX)	0024_{16}	FF_{16}
(27)	Timer X (TX)	0025_{16}	FF_{16}
(28)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(29)	Timer Y (TY)	0027_{16}	FF_{16}
(30)	Timer count source selection register (TCSS)	0028_{16}	00_{16}
(31)	A-D control register (ADCON)	0034_{16}	0 0 0 1 0 0 0 0
(32)	A-D conversion low-order register (ADL)	0035_{16}	X X X X X X X X
(33)	A-D conversion high-order register (ADH)	0036_{16}	0 0 0 0 0 0 X X
(34)	MISRG	0038_{16}	00_{16}
(35)	Watchdog timer control register (WDTCON)	0039_{16}	0 0 1 1 1 1 1 1
(36)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(37)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(38)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(39)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(40)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(41)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(42)	Processor status register	(PS)	X X X X X 1 X X
(43)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 38 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3850 group (spec. H) has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.
Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power on and at returning from the stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3•f(XCIN).

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.
The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillation stops. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116." When the oscillation stabilizing time set after STP instruction released bit is "1," set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.
Either XIN or XCIN divided by 16 is input to the prescaler 12 as count source. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.
When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

■Note

When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

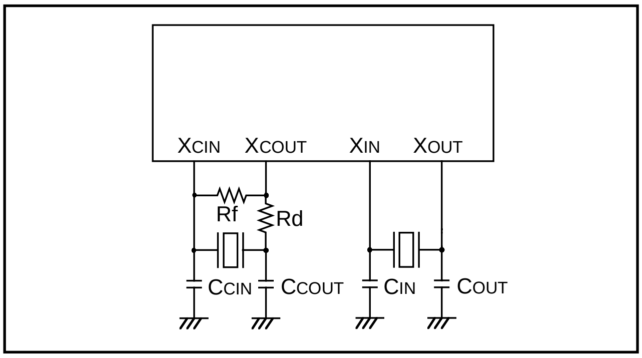


Fig. 39 Ceramic resonator circuit

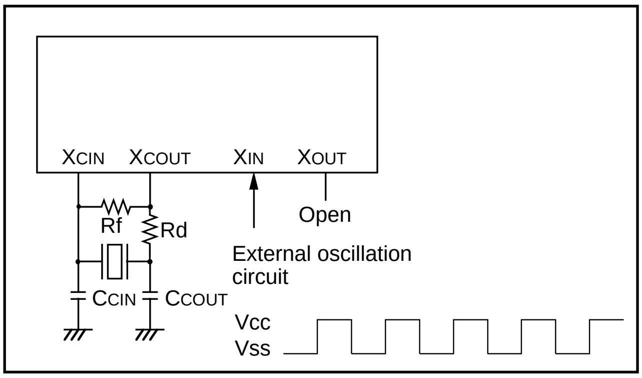
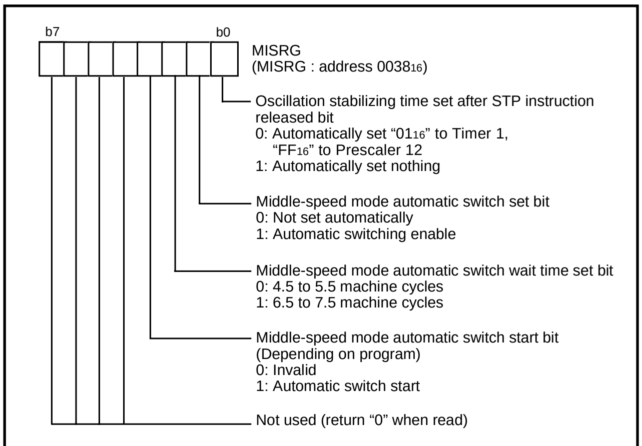


Fig. 40 External clock input circuit

[MISRG (MISRG)] 0038_{16}

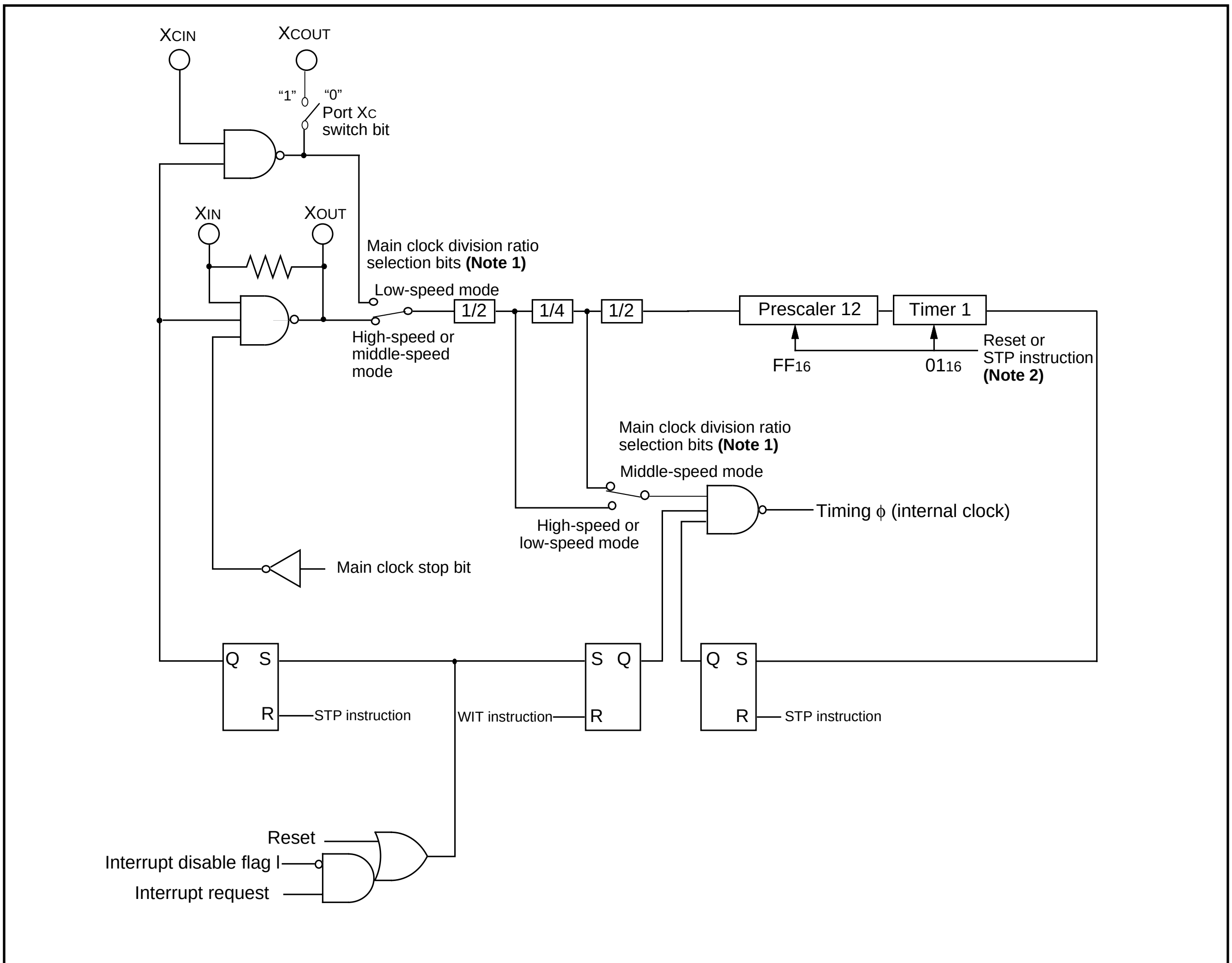
MISRG consists of three control bits (bits 1 to 3) for middle-speed mode automatic switch and one control bit (bit 0) for oscillation stabilizing time set after STP instruction released.

By setting the middle-speed mode automatic switch start bit to “1” while operating in the low-speed mode and setting the middle-speed mode automatic switch set bit to “1”, X_{IN} oscillation automatically starts and the mode is automatically switched to the middle-speed mode.



Note: When the mode is automatically switched from the low-speed mode to the middle-speed mode, the value of CPU mode register (address $003B_{16}$) changes.

Fig. 41 Structure of MISRG

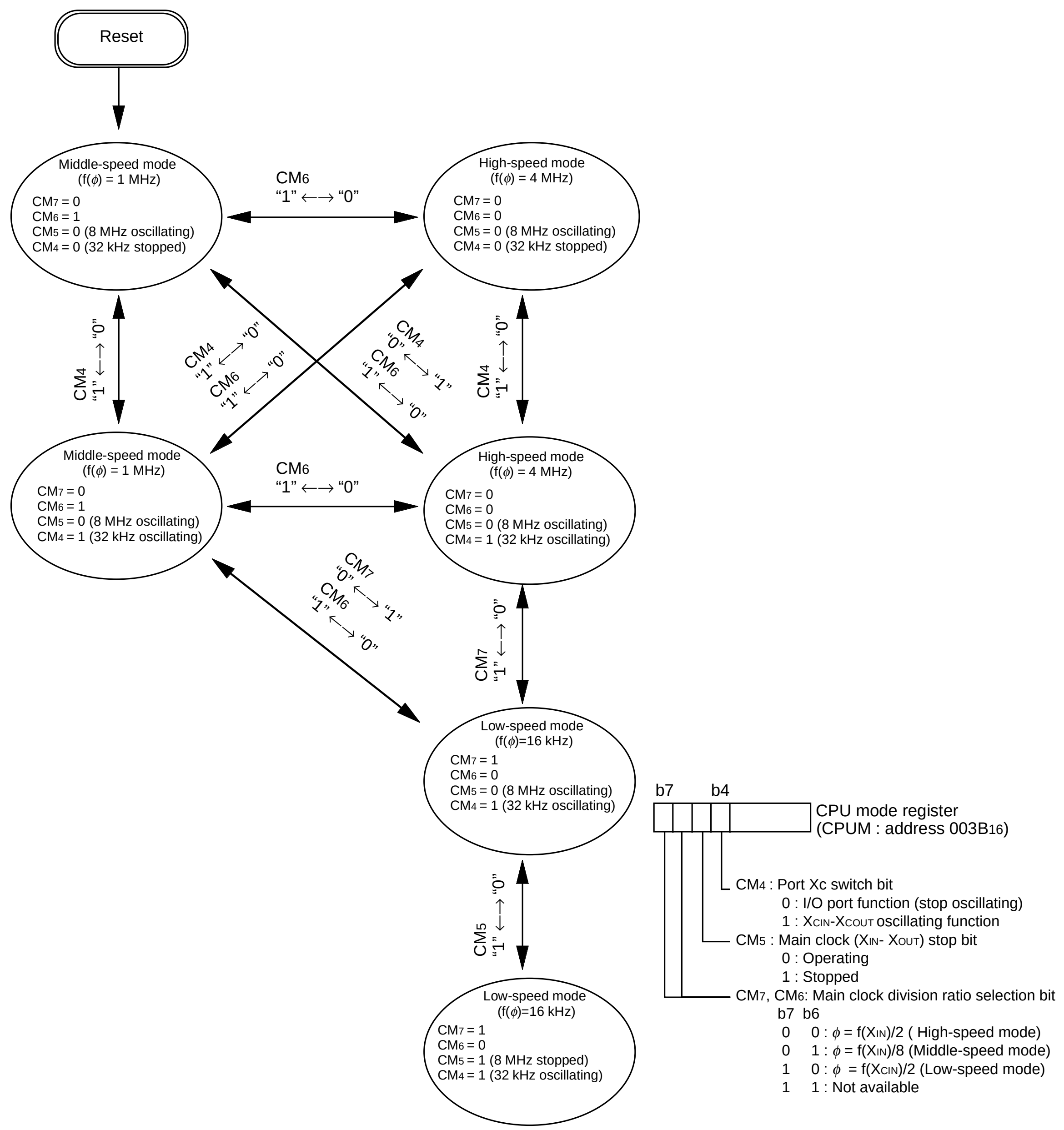


Notes 1: Any one of high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port Xc switch bit (b4) to “1”.

2: When bit 0 of MISRG = “0”

Fig. 42 System clock generating circuit block diagram (Single-chip mode)

MITSUBISHI ELECTRIC



Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)

2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.

3 : Timer operates in the wait mode.

4 : When bit 0 of MISRG is "0" and the stop mode is ended, a delay of approximately 1 ms occurs by connecting timer 1 in middle/high-speed mode.

5 : When bit 0 of MISRG is "0" and the stop mode is ended, the following is performed.
(1) After the clock is restarted, a delay of approximately 256 ms occurs in low-speed mode if Timer 12 count source selection bit is "0".
(2) After the clock is restarted, a delay of approximately 16 ms occurs in low-speed mode if Timer 12 count source selection bit is "1".

6 : Wait until oscillation stabilizes after oscillating the main clock X_{IN} before the switching from the low-speed mode to middle/high-speed mode.

7 : The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. ϕ indicates the internal clock.

Fig. 43 State transitions of system clock

FLASH MEMORY VERSION
Summary

Table 9 shows the summary of the M38507F8 (flash memory version).

Table 9 Summary of M38507F8 (flash memory version)

Item		Specification
Power source voltage		Vcc = 2.7–5.5 V **(Note 1)** Vcc = 2.7–3.6 V **(Note 2)**
Program/Erase VPP voltage		4.5–5.5 V, f(XIN) = 8 MHz
Flash memory mode		3 modes (Parallel I/O mode, Standard serial I/O mode, CPU rewrite mode)
Erase block division	User ROM area	1 block (32 Kbytes)
	Boot ROM area	1 block (4 Kbytes) **(Note 3)**
Program method		Byte program
Erase method		Batch erasing
Program/Erase control method		Program/Erase control by software command
Number of commands		6 commands
Number of program/Erase times		100 times
ROM code protection		Available in parallel I/O mode, and standard serial I/O mode

Notes 1: The power source voltage must be Vcc = 4.5–5.5 V at program and erase operation.
2: The power source voltage can be Vcc = 3.0–3.6 V also at program and erase operation.
3: The Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. This Boot ROM area can be rewritten in only parallel I/O mode.

Flash Memory Mode

The M38507F8 (flash memory version) has an internal new DINOR (DIvided bit line NOR) flash memory that can be rewritten with a single power source when V_{CC} is 5 V, and 2 power sources when V_{CC} is 3.3 V.

For this flash memory , three flash memory modes are available in which to read, program, and erase: parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and a CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU). Each mode is detailed in the pages to follow.

The flash memory of the M38507F8 is divided into User ROM area and Boot ROM area as shown in Figure 44.

In addition to the ordinary user ROM area to store a microcomputer operation control program, the flash memory has a Boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

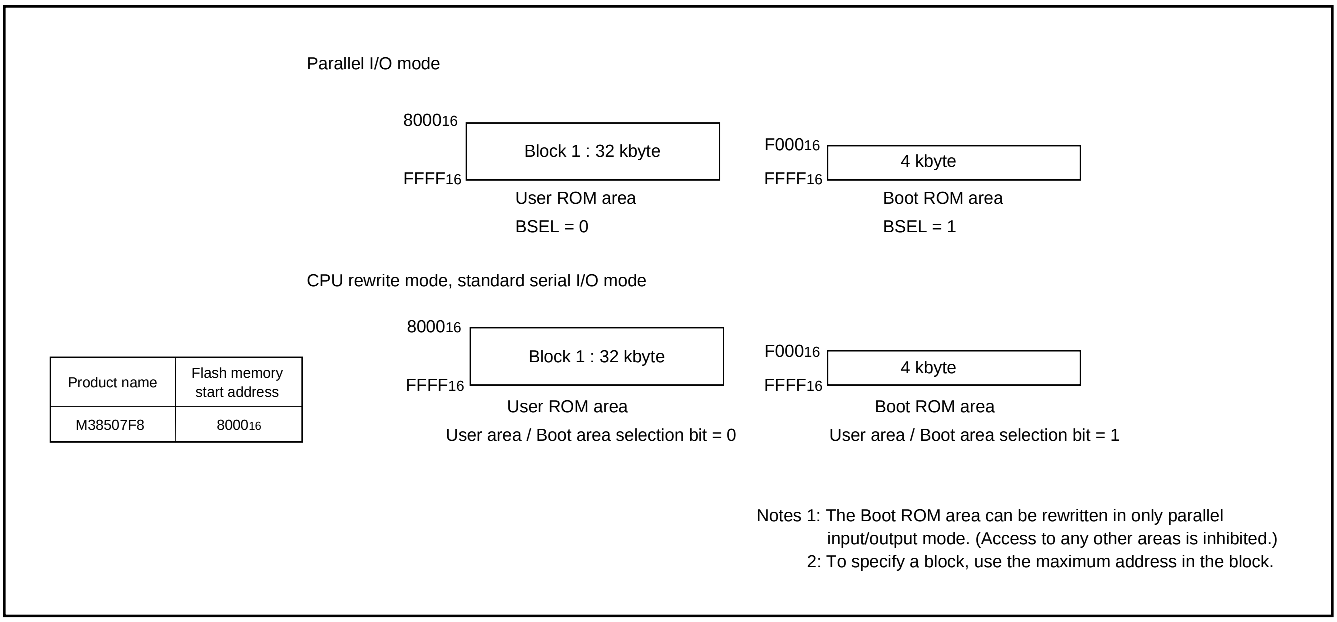


Fig. 44 Block diagram of flash memory version

CPU Rewrite Mode

In CPU rewrite mode, the on-chip flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).
In CPU rewrite mode, only the user ROM area shown in Figure 44 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the user ROM area and each block area.
The control program for CPU rewrite mode can be stored in either user ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area before it can be executed.

Microcomputer Mode and Boot Mode

The control program for CPU rewrite mode must be written into the user ROM or Boot ROM area in parallel I/O mode beforehand. (If the control program is written into the Boot ROM area, the standard serial I/O mode becomes unusable.)
See Figure 44 for details about the Boot ROM area.
Normal microcomputer mode is entered when the microcomputer is reset with pulling CNV_{SS} pin low. In this case, the CPU starts operating using the control program in the user ROM area.
When the microcomputer is reset by pulling the $P4_1/INT_0$ pin high, the CNV_{SS} pin high, the CPU starts operating using the control program in the Boot ROM area (program start address is $FFFC_{16}$, $FFFD_{16}$ fixation). This mode is called the “boot” mode.

Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command. In case of the M38507F8, it has only one block.

Outline Performance (CPU Rewrite Mode)

In the CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This rewrite control program must be transferred to internal RAM before it can be executed.
The CPU rewrite mode is accessed by applying 5V ± 10% to the CNV_{SS} pin and writing “1” for the CPU rewrite mode select bit (bit 1 in address $0FFE_{16}$). Software commands are accepted once the mode is accessed.
Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.
Figure 45 shows the flash memory control register.
Bit 0 is the RY/$\overline{BY}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is “0”. Otherwise, it is “1”.
Bit 1 is the CPU rewrite mode select bit. When this bit is set to “1” and 5V ± 10% are applied to the CNV_{SS} pin, the M38507F8 accesses the CPU rewrite mode. Software commands are accepted once the mode is accessed. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in RAM for write to bit 1. To set this bit to “1”, it is necessary to write “0” and then write “1” in succession. The bit can be set to “0” by only writing a “0”.
Bit 2 is the CPU rewrite mode entry flag. This bit can be read to check whether the CPU rewrite mode has been entered or not.
Bit 3 is the flash memory reset bit used to reset the control circuit of the internal flash memory. This bit is used when exiting CPU rewrite mode and when flash memory access has failed. When the CPU rewrite mode select bit is “1”, writing “1” for this bit resets the control circuit. To release the reset, it is necessary to set this bit to “0”.
Bit 4 is the User area/Boot area selection bit. When this bit is set to “1”, Boot ROM area is accessed, and CPU rewrite mode in Boot ROM area is available. In boot mode, this bit is set “1” automatically. Operation of this bit must be in RAM area.
Figure 46 shows a flowchart for setting/releasing the CPU rewrite mode.

Precautions on CPU Rewrite Mode

Described below are the precautions to be observed when rewriting the flash memory in CPU rewrite mode.

(1) Operation speed

During CPU rewrite mode, set the internal clock frequency 4MHz or less using the main clock division ratio selection bits (bit 6, 7 at $003B_{16}$).

(2) Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode .

(3) Interrupts inhibited against use

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

(4) Watchdog timer

In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

(5) Reset

Reset is always valid. In case of CNV_{SS} = H when reset is released, boot mode is active. So the program starts from the address contained in address $FFFC_{16}$ and $FFFD_{16}$ in boot ROM area.

Flash memory control register

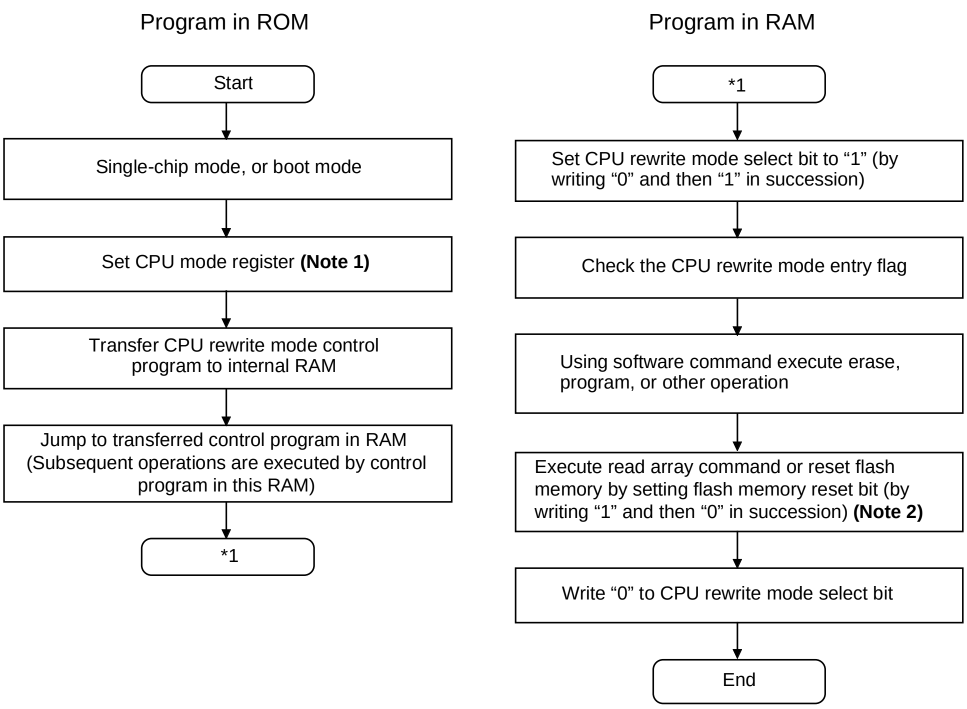
b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	When reset
FMCR	0FFE16	XXX00001

Bit symbol	Bit name	Function	R	W
FMCR0	RY/$\overline{BY}$ status flag	0: Busy (being written or erased) 1: Ready	○	—
FMCR1	CPU rewrite mode select bit (Note 1)	0: Normal mode (Software commands invalid) 1: CPU rewrite mode (Software commands acceptable)	○	○
FMCR2	CPU rewrite mode entry flag	0: Normal mode (Software commands invalid) 1: CPU rewrite mode (Software commands acceptable)	○	—
FMCR3	Flash memory reset bit (Note 2)	0: Normal operation 1: Reset	○	○
FMCR4	User area / Boot area selection bit	0: User ROM area 1: Boot ROM area	○	○
	Nothing is assigned. When write, set “0”. When read, values are indeterminate.		—	—

Notes 1: For this bit to be set to “1”, the user needs to write a “0” and then a “1” to it in succession.
2: Effective only when the CPU rewrite mode select bit = 1. Set this bit to “0” subsequently after setting it to “1” (reset).

Fig. 45 Flash memory control registers



Notes 1: Set bit 6, 7 (Main clock division ratio selection bits) at CPU mode register (003B16).
2: Before exiting the CPU rewrite mode after completing erase or program operation, always be sure to execute a read array command or reset the flash memory.

Fig. 46 CPU rewrite mode set/reset flowchart

Software Commands

Table 10 lists the software commands.
After setting the CPU rewrite mode select bit to “1”, write a software command to specify an erase or program operation.
The content of each software command is explained below.

Read Array Command (FF_{16})

The read array mode is entered by writing the command code “FF_{16}” in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the content of the specified address is read out at the data bus (D_0–D_7).
The read array mode is retained intact until another command is written. And after power on and after recover from deep power down mode, this mode is selected also.

Read Status Register Command (70_{16})

When the command code “70_{16}” is written in the first bus cycle, the content of the status register is read out at the data bus (D_0–D_7) by a read in the second bus cycle.
The status register is explained in the next section.

Clear Status Register Command (50_{16})

This command is used to clear the bits SR1,SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code “50_{16}” in the first bus cycle.

Table 10 List of software commands (CPU rewrite mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X **(Note 4)**	FF_{16}			
Read status register	2	Write	X	70_{16}	Read	X	SRD **(Note 1)**
Clear status register	1	Write	X	50_{16}			
Program	2	Write	X	40_{16}	Write	WA **(Note 2)**	WD **(Note 2)**
Erase all block	2	Write	X	20_{16}	Write	X	20_{16}
Block erase	2	Write	X	20_{16}	Write	BA **(Note 3)**	$D0_{16}$

Notes 1: SRD = Status Register Data
2: WA = Write Address, WD = Write Data
3: BA = Block Address (Enter the maximum address of each block.)
4: X denotes a given address in the user ROM area .

Program Command (40_{16})

Program operation starts when the command code "40_{16}" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.
Whether the write operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ status flag. When the program starts, the read status register mode is accessed automatically and the content of the status register is read into the data bus (D0–D7). The status register bit 7 (SR7) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF_{16}) is written.
The RY/$\overline{BY}$ status flag is "0" during write operation and "1" when the write operation is completed as is the status register bit 7.
At program end, program results can be checked by reading the status register.

Erase All Blocks Command (20_{16}/20_{16})

By writing the command code "20_{16}" in the first bus cycle and the confirmation command code "20_{16}" in the second bus cycle that follows, the system starts erase all blocks(erase and erase verify).
Whether the erase all blocks command is terminated can be confirmed by reading the status register or the RY/$\overline{BY}$ status flag. When the erase all blocks operation starts, the read status register mode is accessed automatically and the content of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the erase operation starts and is returned to "1" upon completion of the erase operation. In this case, the read status register mode remains active until the read array command (FF_{16}) is written.
The RY/$\overline{BY}$ status flag is "0" during erase operation and "1" when the erase operation is completed as is the status register bit 7.
At erase all blocks end, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

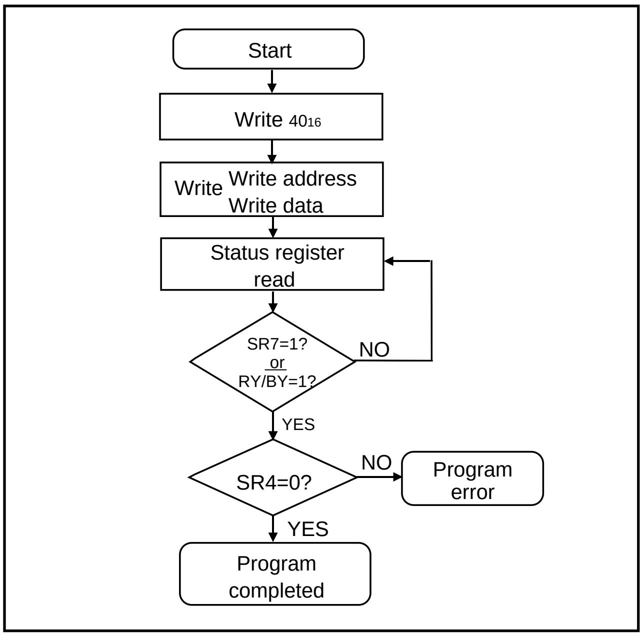


Fig. 47 Program flowchart

Block Erase Command (20_{16}/$D0_{16}$)

By writing the command code "20_{16}" in the first bus cycle and the confirmation command code "$D0_{16}$" in the second bus cycle that follows to the block address of a flash memory block, the system initiates a block erase (erase and erase verify) operation.
Whether the block erase operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ status flag. At the same time the block erase operation starts, the read status register mode is automatically entered, so the content of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF_{16}) is written.
The RY/$\overline{BY}$ status flag is "0" during block erase operation and "1" when the block erase operation is completed as is the status register bit 7.
After the block erase operation is completed, the status register can be read out to know the result of the block erase operation. For details, refer to the section where the status register is detailed.

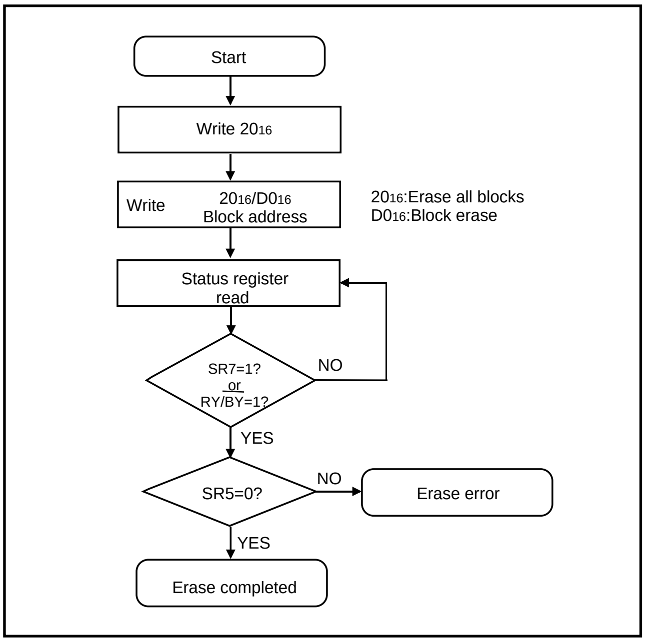


Fig. 48 Erase flowchart

Status Register

The status register shows the operating state of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways.

(1) By reading an arbitrary address from the user ROM area after writing the read status register command (70_{16})

(2) By reading an arbitrary address from the user ROM area in the period from when the program starts or erase operation starts to when the read array command (FF_{16}) is input

Table 11 shows the status register.
Also, the status register can be cleared in the following way.
(1) By writing the clear status register command (50_{16})
(2) In the deep power down mode
(3) In the power supply off state
After a reset, the status register is set to "80_{16}".
Each bit in this register is explained below.

Sequencer status (SR7)

After power-on, and after recover from deep power down mode, the sequencer status is set to "1"(ready).
The sequencer status indicates the operating status of the device. This status bit is set to "0" (busy) during write or erase operation and is set to "1" upon completion of these operations.

Erase status (SR5)

The erase status informs the operating status of erase operation to the CPU. When an erase error occurs, it is set to "1".
The erase status is reset to "0" when cleared.

Program status (SR4)

The program status informs the operating status of write operation to the CPU. When a write error occurs, it is set to "1".
The program status is reset to "0" when cleared.

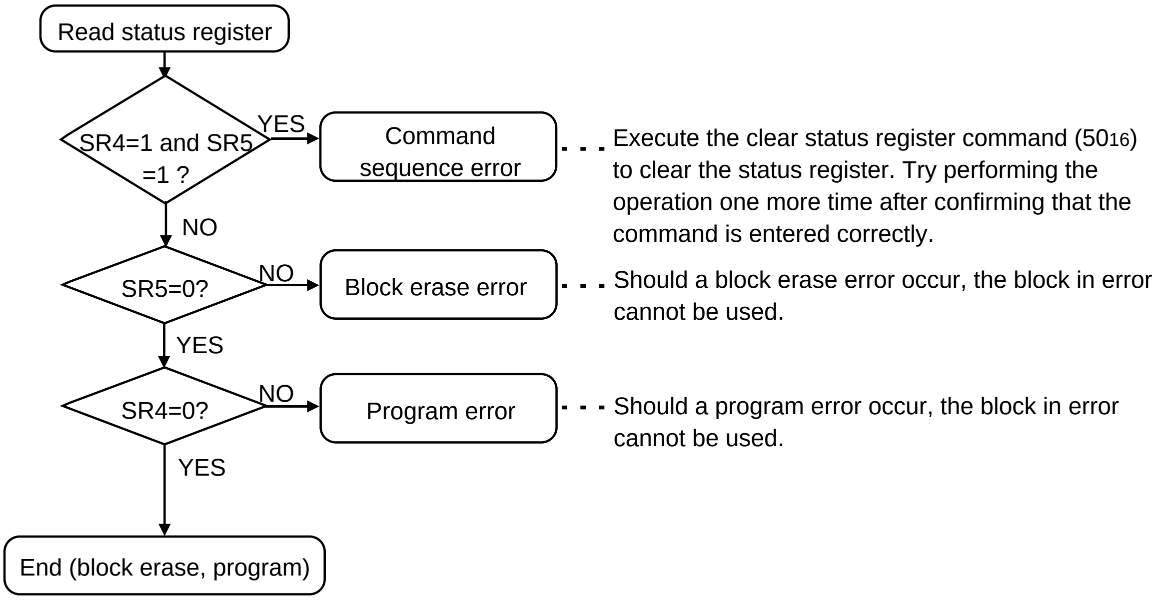
If "1" is written for any of the SR5 or SR4 bits, the program, erase all blocks, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.
Also, any commands are not correct, both SR5 and SR4 are set to "1".

Table 11 Definition of each bit in status register

Each bit of SRD0 bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 49 shows a full status check flowchart and the action to be taken when each error occurs.



Note: When one of SR5 to SR4 is set to “1” , none of the program, erase all blocks, and block erase commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 49 Full status check flowchart and remedial procedure for errors

Functions To Inhibit Rewriting Flash Memory Version

To prevent the contents of the flash memory version from being read out or rewritten easily, the device incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

ROM code protect function

The ROM code protect function is the function inhibit reading out or modifying the contents of the flash memory version by using the ROM code protect control address ($FFDB_{16}$) during parallel I/O mode. Figure 50 shows the ROM code protect control address ($FFDB_{16}$). (This address exists in the user ROM area.)

If one of the pair of ROM code protect bits is set to “0”, ROM code protect is turned on, so that the contents of the flash memory version are protected against readout and modification. ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM code protect reset bits are set to “00”, ROM code protect is turned off, so that the contents of the flash memory version can be read out or modified. Once ROM code protect is turned on, the contents of the ROM code protect reset bits cannot be modified in parallel I/O mode. Use the serial I/O or some other mode to rewrite the contents of the ROM code protect reset bits.

ROM code protect control address

b7 b6 b5 b4 b3 b2 b1 b0 : [ ] [ ] [ ] [ ] [ ] [ ] [1] [1]

Symbol	Address	When reset
ROMCP	$FFDB_{16}$	FF_{16}

Bit symbol	Bit name	Function
Reserved bit		Always set this bit to “1”
ROMCP2	ROM code protect level 2 set bit **(Note 1, 2)**	b3 b2 00: Protect enabled 01: Protect enabled 10: Protect enabled 11: Protect disabled
ROMCR	ROM code protect reset bit **(Note 3)**	b5 b4 00: Protect removed 01: Protect set bit effective 10: Protect set bit effective 11: Protect set bit effective
ROMCP1	ROM code protect level 1 set bit **(Note 1)**	b7 b6 00: Protect enabled 01: Protect enabled 10: Protect enabled 11: Protect disabled

Notes 1: When ROM code protect is turned on, the on-chip flash memory is protected against readout or modification in parallel input/output mode.
2: When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.
3: The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2. However, since these bits cannot be changed in parallel input/output mode, they need to be rewritten in serial input/output mode or some other mode.

Fig. 50 ROM code protect control address

ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the peripheral unit is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the peripheral unit are not accepted. The ID code consists of 8-bit data, the areas of which are $FFD4_{16}$ to $FFDA_{16}$. Write a program which has had the ID code preset at these addresses to the flash memory.

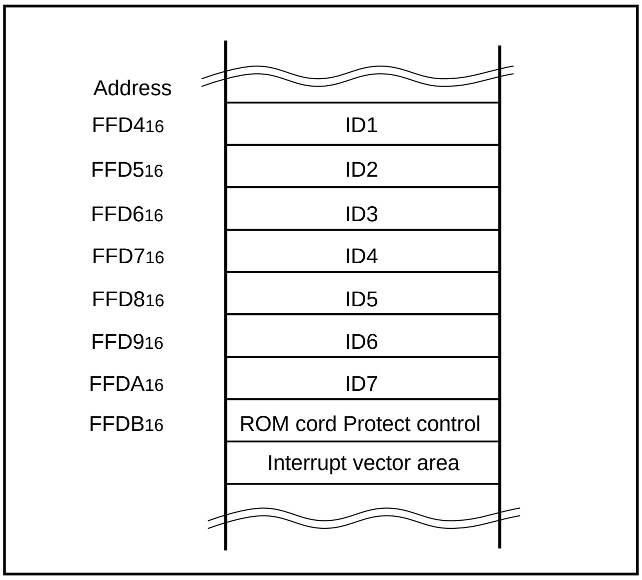


Fig. 51 ID code store addresses

Parallel I/O Mode

The parallel I/O mode is entered by making connections shown in Figure 52 and then turning the Vcc power supply on.

Address

The user ROM is only one block as shown in Figure 44. The block address referred to in this data sheet is the maximum address value of each block.

User ROM and Boot ROM Areas

In parallel I/O mode, the user ROM and boot ROM areas shown in Figure 44 can be rewritten. The BSEL pin is used to choose between these two areas. The user ROM area is selected by pulling the BSEL input low; the boot ROM area is selected by driving the BSEL input high. Both areas of flash memory can be operated on in the same way.
Program and block erase operations can be performed in the user ROM area. The user ROM area and its block is shown in Figure 44.
The user ROM area is 32 Kbytes in size. In parallel I/O mode, it is located at addresses 8000_{16} through $FFFF_{16}$. The boot ROM area is 4 Kbytes in size. In parallel I/O mode, it is located at addresses $F000_{16}$ through $FFFF_{16}$. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)
In the Boot ROM area, an erase block operation is applied to only one 4 Kbyte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the Mitsubishi factory. Therefore, using the device in standard serial input/output mode, you do not need to write to the boot ROM area.

Functional Outline (Parallel I/O Mode)

In parallel I/O mode, bus operation modes—Read, Output Disable, Standby, Write, and Deep Power Down—are selected by the status of the $\overline{CE}$, $\overline{OE}$, $\overline{WE}$, and $\overline{RP}$ input pins.
The contents of erase, program, and other operations are selected by writing a software command. The data, status register, etc. in memory can only be read out by a read after software command input.
Program and erase operations are controlled using software commands.
The following explains about bus operation modes, software commands, and status register.

Bus Operation Modes

Read

The Read mode is entered by pulling the $\overline{OE}$ pin low when the $\overline{CE}$ pin is low and the $\overline{WE}$ and $\overline{RP}$ pins are high. There are two read modes: array, and status register, which are selected by software command input. In read mode, the data corresponding to each software command entered is output from the data I/O pins D_0–D_7. The read array mode is automatically selected when the device is powered on or after it exits deep power down mode.

Output Disable

The output disable mode is entered by pulling the $\overline{CE}$ pin low and the $\overline{WE}$, $\overline{OE}$, and $\overline{RP}$ pins high. Also, the data I/O pins are placed in the high-impedance state.

Standby

The standby mode is entered by driving the $\overline{CE}$ pin high when the $\overline{RP}$ pin is high. Also, the data I/O pins are placed in the high-impedance state. However, if the $\overline{CE}$ pin is set high during erase or program operation, the internal control circuit does not halt immediately and normal power consumption is required until the operation under way is completed.

Write

The write mode is entered by pulling the $\overline{WE}$ pin low when the $\overline{CE}$ pin is low and the $\overline{OE}$ and $\overline{RP}$ pins are high. In this mode, the device accepts the software commands or write data entered from the data I/O pins. A program, erase, or some other operation is initiated depending on the content of the software command entered here. The input data such as address and software command is latched at the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs earlier.

Deep Power Down

The deep power down is entered by pulling the $\overline{RP}$ pin low. Also, the data I/O pins are placed in the high-impedance state. When the device is freed from deep power down mode, the read array mode is selected and the content of the status register is set to "80_{16}." If the $\overline{RP}$ pin is pulled low during erase or program operation, the operation under way is canceled and the data in the relevant block becomes invalid.

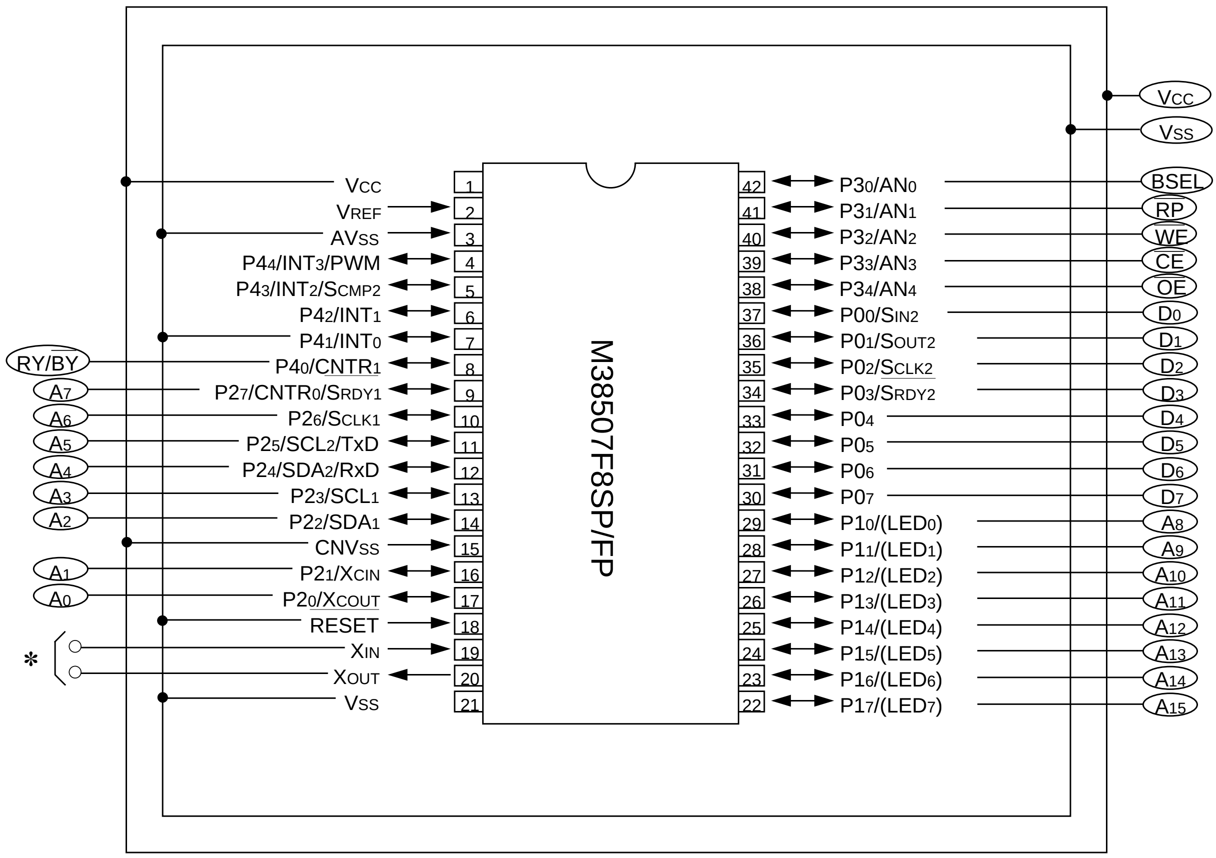
Table 12 Relationship between control signals and bus operation modes

Mode \ Pin name		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RP}$	D_0 to D_7
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data output
	Status register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Status register data output
Output disabled		V_{IL}	V_{IH}	V_{IH}	V_{IH}	High impedance
Stand by		V_{IH}	X	X	V_{IH}	High impedance
Write	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command/data input
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command input
	Other	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command input
Deep power down		X	X	X	V_{IL}	High impedance

Note : X can be V_{IL} or V_{IH}.

Table 13 Description of Pin Function (Flash Memory Parallel I/O Mode)

Pin name	Signal name	I/O	Function
V_{CC},V_{SS}	Power supply input	I	Apply 5.0 ± 0.5 V to the Vcc pin and 0 V to the Vss pin.
CNV_{SS}	CNV_{SS}	I	Connect this pin to V_{CC}.
$\overline{RESET}$	Reset input	I	Reset input pin. When reset is held low, more than 20 cycles of clock are required at the X_{IN} pin.
X_{IN}	Clock input	I	Connect a ceramic or crystal resonator between the X_{IN} and X_{OUT} pins. When entering an externally drived clock, enter it from X_{IN} and leave X_{OUT} open.
X_{OUT}	Clock output	O	
AV_{SS}	Analog power supply input	I	Connect AVss to Vss.
V_{REF}	Reference voltage input	I	Input AD reference voltage or keep open.
$P0_0$ to $P0_7$	Data I/O D_0 to D_7	I/O	These are data D_0–D_7 input/output pins.
$P1_0$ to $P1_7$	Address input A_8 to A_{15}	I	These are address A_8–A_{15} input pins.
$P2_0$ to $P2_7$	Address input A_0 to A_7	I	These are address A_0–A_7 input pins.
$P3_0$	BSEL input	I	This is a BSEL input pin.
$P3_1$	$\overline{RP}$ input	I	This is a $\overline{RP}$ input pin.
$P3_2$	$\overline{WE}$ input	I	This is a $\overline{WE}$ input pin.
$P3_3$	$\overline{CE}$ input	I	This is a $\overline{CE}$ input pin.
$P3_4$	$\overline{OE}$ input	I	This is a $\overline{OE}$ input pin.
$P4_0$	RY/$\overline{BY}$ output	O	This is a RY/$\overline{BY}$ output pin.
$P4_1$	Input $P4_1$	I	Enter low signals to this pin.
$P4_2$ to $P4_4$	Input P4	I	Input “H” or “L” or keep open.



Mode setup method

Signal	Value
CNVss	Vcc
P41/INT0	Vss
RESET	Vss

✻ Connect oscillator circuit

Fig. 52 Pin connection diagram in parallel I/O mode

Software Commands

Table 14 lists the software commands. By entering a software command from the data I/O pins (D_0–D_7) in Write mode, specify the content of the operation, such as erase or program operation, to be performed.
The following explains the content of each software command.

Read Array Command (FF_{16})

The read array mode is entered by writing the command code "FF_{16}" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the content of the specified address is output from the data I/O pins (D_0–D_7).
The read array mode is retained intact until another command is written.
The read array mode is also selected automatically when the device is powered on and after it exits deep power down mode.

Read Status Register Command (70_{16})

When the command code "70_{16}" is written in the first bus cycle, the content of the status register is output from the data I/O pins (D_0–D_7) by a read in the second bus cycle. Since the content of the status register is updated at the falling edge of $\overline{OE}$ or $\overline{CE}$, the $\overline{OE}$ or $\overline{CE}$ signal must be asserted each time the status is read. The status register is explained in the next section.

Clear Status Register Command (50_{16})

This command is used to clear the bits SR4,SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50_{16}" in the first bus cycle.

Table 14 Software command list (parallel I/O mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X(Note 4)	FF_{16}			
Read status register	2	Write	X	70_{16}	Read	X	SRD(Note 1)
Clear status register	1	Write	X	50_{16}			
Program	2	Write	X	40_{16}	Write	WA(Note 2)	WD(Note 2)
All block erase	2	Write	X	20_{16}	Write	X	20_{16}
Block erase	2	Write	X	20_{16}	Write	BA(Note 3)	$D0_{16}$

Notes 1: SRD = Status Register Data
2: WA = Write Address, WD = Write Data
3: BA = Block Address (Enter the maximum address of each block)
4: X denotes a given address in the user ROM area or boot ROM area.

Program Command (40$_{16}$)

The program operation starts when the command code "40$_{16}$" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.
Whether the write operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ signal status. When the program starts, the read status register mode is accessed automatically and the content of the status register can be read out from the data bus (D_0–D_7). The status register bit 7 (SR7) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF$_{16}$) is written.
The RY/$\overline{BY}$ pin is "L" during write operation and "H" when the write operation is completed as is the status register bit 7.
At program end, program results can be checked by reading the status register.

Erase All Blocks Command (20$_{16}$/20$_{16}$)

By writing the command code "20$_{16}$" in the first bus cycle and the confirmation command code "20$_{16}$" in the second bus cycle that follows, the system starts erase all blocks(erase and erase verify).
Whether the erase all blocks command is terminated can be confirmed by reading the status register or the RY/$\overline{BY}$ signal status . When the erase all blocks operation starts, the read status register mode is accessed automatically and the content of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the erase operation starts and is returned to "1" upon completion of the erase operation. In this case, the read status register mode remains active until the read array command (FF$_{16}$) is written.
The RY/$\overline{BY}$ pin is "L" during erase operation and "H" when the erase operation is completed as is the status register bit 7.
At erase all blocks end, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

Block Erase Command (20$_{16}$/D0$_{16}$)

By writing the command code "20$_{16}$" in the first bus cycle and the confirmation command code "D0$_{16}$" in the second bus cycle that follows to the block address of a flash memory block, the system initiates a block erase (erase and erase verify) operation.
Whether the block erase operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ signal. At the same time the block erase operation starts, the read status register mode is automatically entered, so the content of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF$_{16}$) is written.
The RY/$\overline{BY}$ pin is "L" during block erase operation and "H" when the block erase operation is completed as is the status register bit 7.
After the block erase operation is completed, the status register can be read out to know the result of the block erase operation. For details, refer to the section where the status register is detailed.

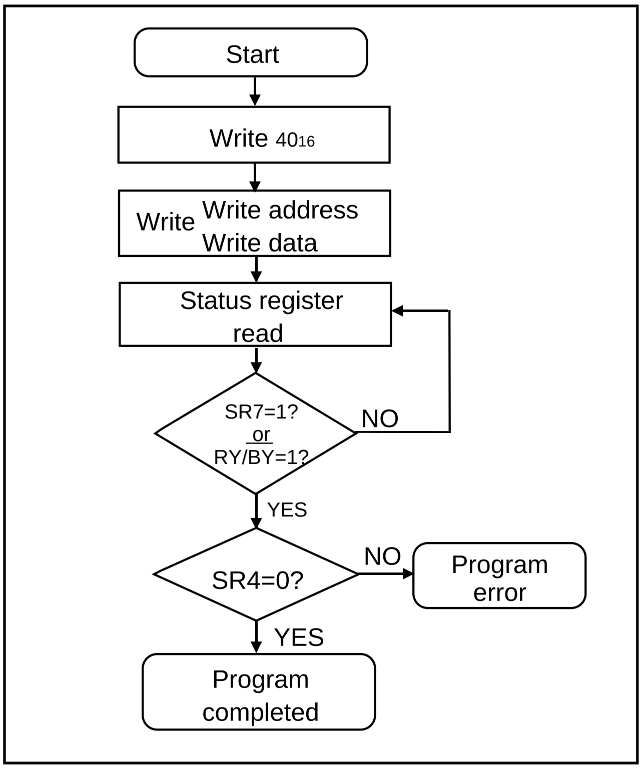


Fig. 53 Page program flowchart

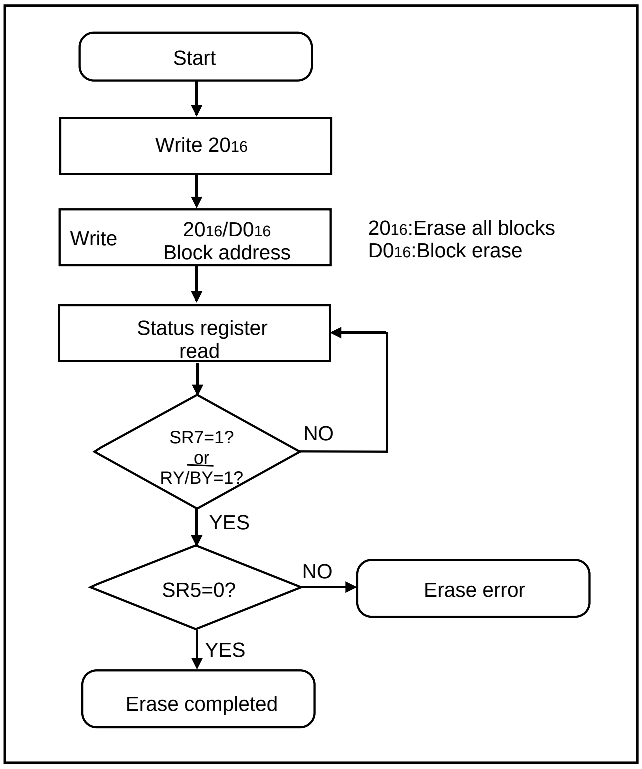


Fig. 54 Block erase flowchart

Status Register

The status register indicates status such as whether an erase operation or a program ended successfully or in error. It can be read under the following conditions.

(1) In the read array mode when the read status register command (70_{16}) is written and the block address is subsequently read.

(2) In the period from when the program write or auto erase starts to when the read array command (FF_{16})

The status register is cleared in the following situations.

(1) By writing the clear status register command (50_{16})

(2) In the deep power down mode

(3) In the power supply off state

Table 15 gives the definition of each status register bit. When power is turned on or returning from the deep power down mode, the status register outputs "80_{16}".

Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory. When power is turned on or returning from the deep power down mode, "1" is set for it. This bit is "0" (busy) during the write or erase operations and becomes "1" when these operations ends.

Erase Status (SR5)

The erase status reports the operating status of the erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

Program Status (SR4)

The program status reports the operating status of the write operation. If a write error occurs, it is set to "1". When the program status is cleared, it is set to "0".

If "1" is written for any of the SR5, SR4 bits, the program erase all blocks, block erase, commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.

Also, any commands are not correct, both SR5 and SR4 are set to "1".

Full Status Check

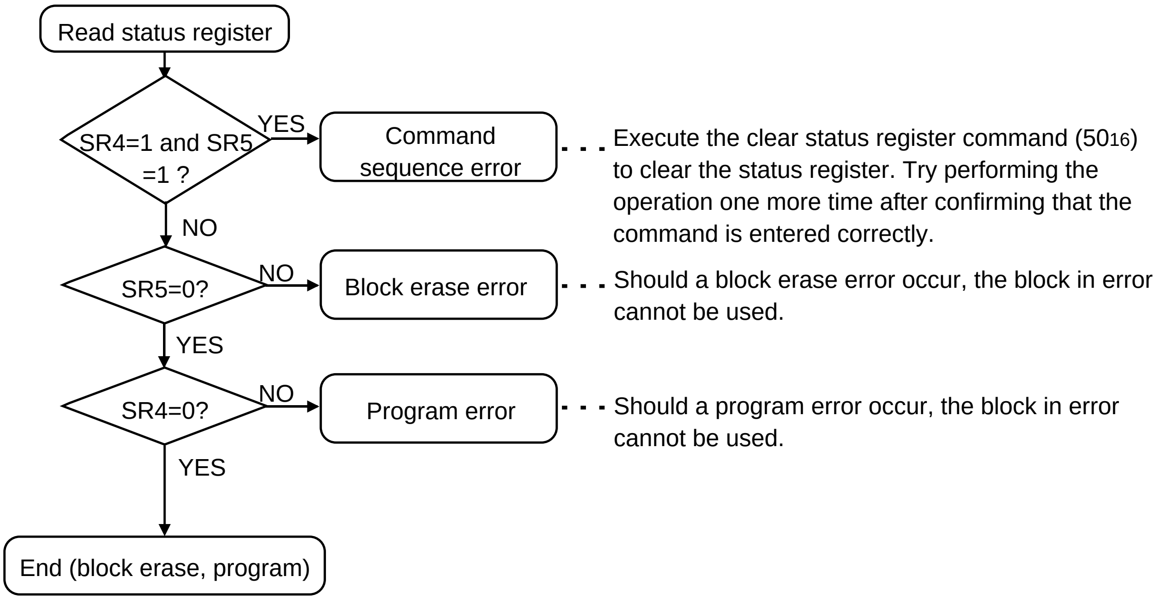
Results from executed erase and program operations can be known by running a full status check. Figure 55 shows a flowchart of the full status check and explains how to remedy errors which occur.

Ready/Busy (RY/$\overline{\text{BY}}$) pin

The RY/$\overline{\text{BY}}$ pin is an output pin (N-chanel open drain output) which, like the sequencer status (SR7), indicates the operating status of the flash memory. It is "L" level during auto program or auto erase operations and becomes to the high impedance state (ready state) when these operations end. The RY/$\overline{\text{BY}}$ pin requires an external pull-up.

Table 15 Status register

Each bit of SRD0 bits	Status name	Definition "1"	Definition "0"
SR7 (D_7)	Sequencer status	Ready	Busy
SR6 (D_6)	Reserved	-	-
SR5 (D_5)	Erase status	Ended in error	Ended successfully
SR4 (D_4)	Program status	Ended in error	Ended successfully
SR3 (D_3)	Reserved	-	-
SR2 (D_2)	Reserved	-	-
SR1 (D_1)	Reserved	-	-
SR0 (D_0)	Reserved	-	-



Note: When one of SR5 to SR4 is set to “1” , none of the program, all blocks erase, or block erase is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 55 Full status check flowchart and remedial procedure for errors

Standard serial I/O mode

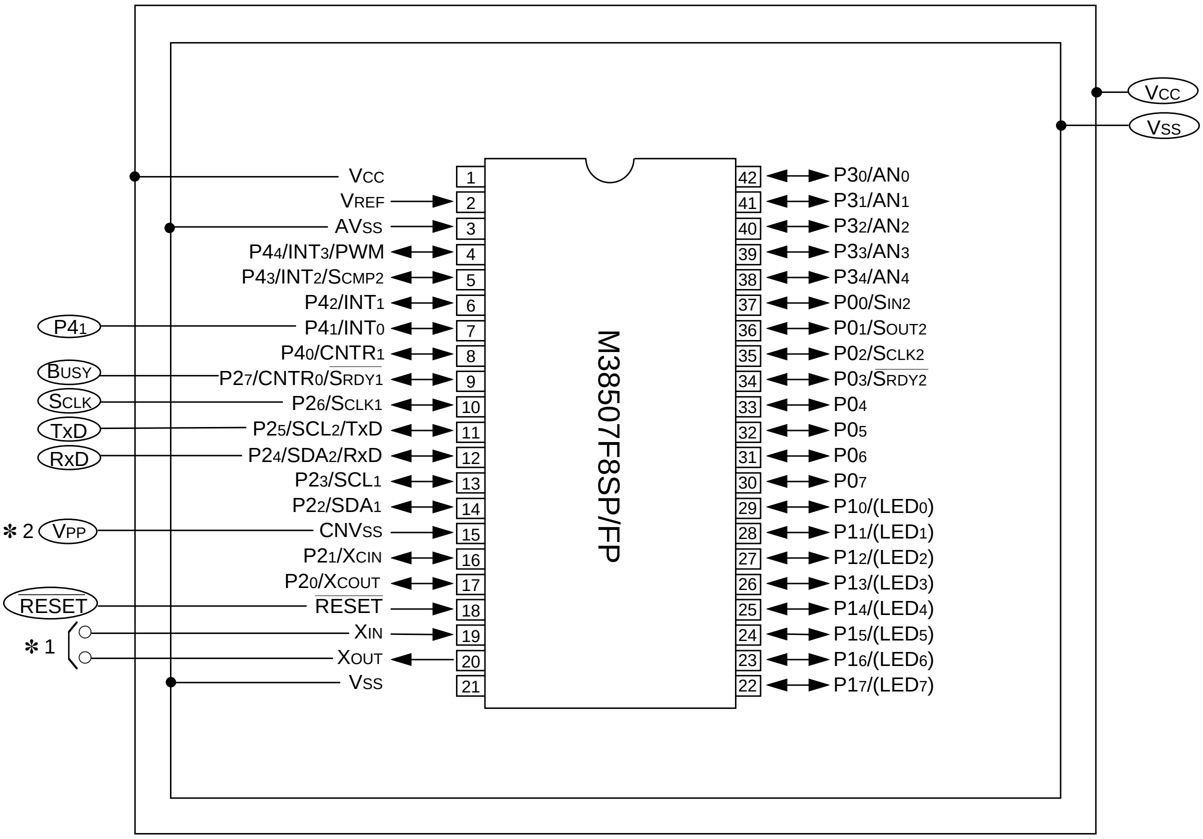
The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This modes require a purpose-specific peripheral unit.
The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU's rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started by connecting “H” to the $P4_1(INT_0)$ pin and “H” to the CNV_{SS} pin (when V_{CC} = 4.5 V to 5.5 V, connect to V_{CC}; when V_{CC} = 2.7 V to 4.5 V, supply 4.5 V to 5.5 V to Vpp from an external source), and releasing the reset operation. (In the ordinary command mode, set CNVss pin to “L” level.)
This control program is written in the boot ROM area when the product is shipped from Mitsubishi. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the boot ROM area is rewritten in the parallel I/O mode. Figure 56 shows the pin connections for the standard serial I/O mode. Serial data I/O uses SI/O1 data serially in 8-bit units.
To use standard serial I/O mode. The operation uses the four SI/O1 pins S_{CLK}, RxD, TxD and $\overline{S_{RDY1}}$ (BUSY). The S_{CLK} pin is the transfer clock input pin through which an external transfer clock is input. The TxD pin is for CMOS output. The $\overline{S_{RDY1}}$ (BUSY) pin outputs an “L” level when ready for reception and an “H” level when reception starts.
In the standard serial I/O mode, only the user ROM area indicated in Figure 44 can be rewritten. The boot ROM cannot.
In the standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

Overview of standard serial I/O mode

In standard serial I/O mode, software commands, addresses and data are input and output between the MCU and peripheral units (serial programer, etc.) using 4-wire clock-synchronized serial I/O (SI/O1).
In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the S_{CLK} pin, and are then input to the MCU via the RxD pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxD pin.
The TxD pin is for CMOS output. Transfer is in 8-bit units with LSB first.
When busy, such as during transmission, reception, erasing or program execution, the $\overline{S_{RDY1}}$ (BUSY) pin is “H” level. Accordingly, always start the next transfer after the $\overline{S_{RDY1}}$ (BUSY) pin is “L” level.
Also, data and status registers in memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following are explained software commands, status registers, etc.

Table 16 Pin functions (Flash memory standard serial I/O mode)

Pin	Name	I/O	Description
V_{CC},V_{SS}	Power input		Apply program/erase protection voltage to Vcc pin and 0 V to Vss pin.
CNV_{SS}	CNV_{SS}	I	Connect to V_{CC} when V_{CC} = 4.5 V to 5.5 V. Connect to Vpp (=4.5 V to 5.5 V) when V_{CC} = 2.7 V to 4.5 V.
$\overline{RESET}$	Reset input	I	Reset input pin. While reset is "L" level, a 20 cycle or longer clock must be input to X_{IN} pin.
X_{IN}	Clock input	I	Connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT} pins. To input an externally generated clock, input it to X_{IN} pin and open X_{OUT} pin.
X_{OUT}	Clock output	O	
AV_{SS}	Analog power supply input		Connect AV_{SS} to V_{SS} .
V_{REF}	Reference voltage input	I	Enter the reference voltage for AD from this pin.
$P0_0$ to $P0_7$	Input port P0	I	Input "H" or "L" level signal or open.
$P1_0$ to $P1_7$	Input port P1	I	Input "H" or "L" level signal or open.
$P2_0$ to $P2_3$	Input port P2	I	Input "H" or "L" level signal or open.
$P2_4$	RxD input	I	Serial data input pin
$P2_5$	TxD output	O	Serial data output pin
$P2_6$	S_{CLK} input	I	Serial clock input pin
$P2_7$	BUSY output	O	BUSY signal output pin
$P3_0$ to $P3_4$	Input port P3	I	Input "H" or "L" level signal or open.
$P4_0$, $P4_2$ to $P4_4$	Input port P4	I	Input "H" or "L" level signal or open.
$P4_1$	Input $P4_1$	I	Input "H" level signal, when reset is released.



Mode setup method

Signal	Value
CNVSS	4.5 to 5.5 V
P41	VCC ✻3
RESET	VSS → VCC

Notes 1: Connect oscillator circuit
2: Connect to Vcc when Vcc = 4.5 V to 5.5 V.
Connect to VPP (=4.5 V to 5.5 V) when Vcc = 2.7 V to 4.5 V.
3: It is necessary to apply Vcc only when reset is released.

Fig. 56 Connection for serial I/O mode

Software Commands

Table 17 lists software commands. In the standard serial I/O mode, erase operations, programs and reading are controlled by transferring software commands via the RxD pin. Software commands are explained here below. Basically, the software commands of the standard serial I/O mode is as same as that of the parallel I/O mode, but it is excluded 1 command of block erase, and it is added 3 command of ID check, download function, version data output function.

Table 17 Software commands (Standard serial I/O mode 1)

	Control command	1st byte transfer	2nd byte	3rd byte	4th byte	5th byte	6th byte		When ID is not verified
1	Page read	FF_{16}	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
2	Page program	41_{16}	Address (middle)	Address (high)	Data input	Data input	Data input	Data input to 259th byte	Not acceptable
3	Erase all blocks	$A7_{16}$	$D0_{16}$						Not acceptable
4	Read status register	70_{16}	SRD output	SRD1 output					Acceptable
5	Clear status register	50_{16}							Not acceptable
6	ID check	$F5_{16}$	Address (low)	Address (middle)	Address (high)	ID size	ID1	To ID7	Acceptable
7	Download function	FA_{16}	Size (low)	Size (high)	Check-sum	Data input	To required number of times		Not acceptable
8	Version data output function	FB_{16}	Version data output	Version data output	Version data output	Version data output	Version data output	Version data output to 9th byte	Acceptable

Notes 1: Shading indicates transfer from flash memory microcomputer to peripheral unit. All other data is transferred from the peripheral unit to the flash memory microcomputer.
2: SRD refers to status register data. SRD1 refers to status register 1 data.
3: All commands can be accepted when the flash memory is totally blank.
4: Address high (A_{16} to A_{23}) must be “00_{16}”.

Page Read Command

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

(1) Transfer the "FF_{16}" command code with the 1st byte.

(2) Transfer addresses A_8 to A_{15} and A_{16} to A_{23} ("00_{16}") with the 2nd and 3rd bytes respectively.

(3) From the 4th byte onward, data (D_0–D_7) for the page (256 bytes) specified with addresses A_8 to A_{23} will be output sequentially from the smallest address first in sync with the fall of the clock.

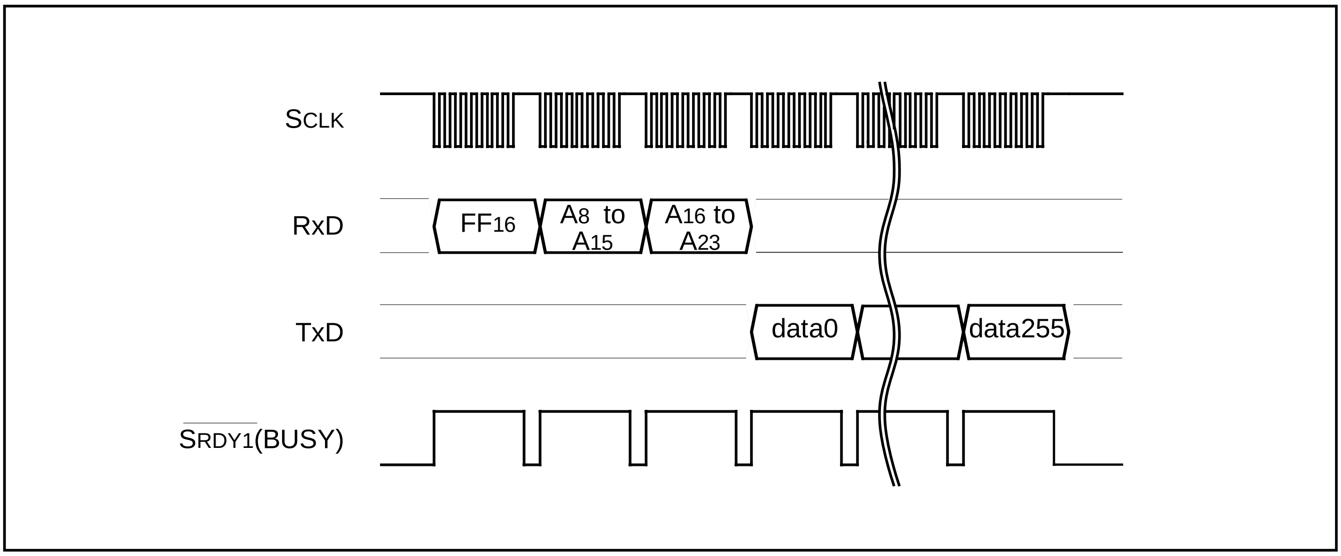


Fig. 57 Timing for page read

Read Status Register Command

This command reads status information. When the "70_{16}" command code is sent with the 1st byte, the contents of the status register (SRD) specified with the 2nd byte and the contents of status register 1 (SRD1) specified with the 3rd byte are read.

Clear Status Register Command

This command clears the bits (SR4–SR5) which are set when the status register operation ends in error. When the "50_{16}" command code is sent with the 1st byte, the aforementioned bits are cleared. When the clear status register operation ends, the $\overline{\text{SRDY1}}$ (BUSY) signal changes from the "H" to the "L" level.

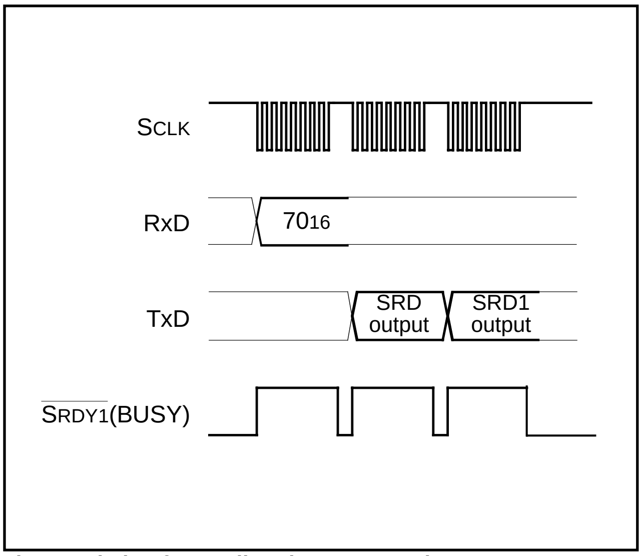


Fig. 58 Timing for reading the status register

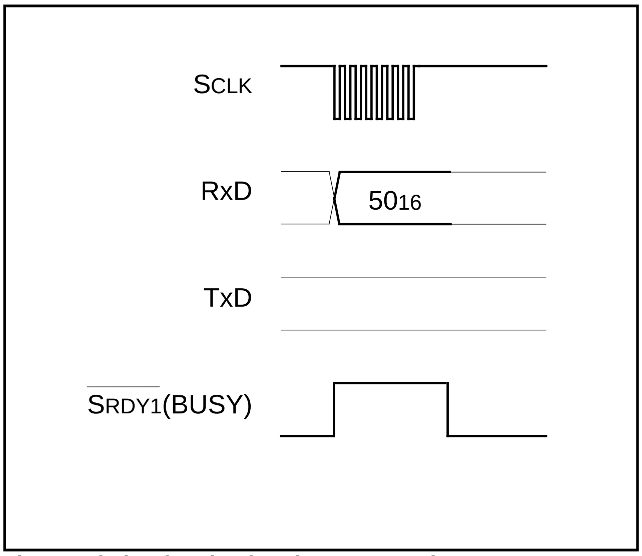


Fig. 59 Timing for clearing the status register

Page Program Command

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

(1) Transfer the “41_{16}” command code with the 1st byte.

(2) Transfer addresses A_8 to A_{15} and A_{16} to A_{23} (“00_{16}”) with the 2nd and 3rd bytes respectively.

(3) From the 4th byte onward, as write data (D_0–D_7) for the page (256 bytes) specified with addresses A_8 to A_{23} is input sequentially from the smallest address first, that page is automatically written.

When reception setup for the next 256 bytes ends, the $\overline{\text{SRDY1}}$ (BUSY) signal changes from the “H” to the “L” level. The result of the page program can be known by reading the status register. For more information, see the section on the status register.

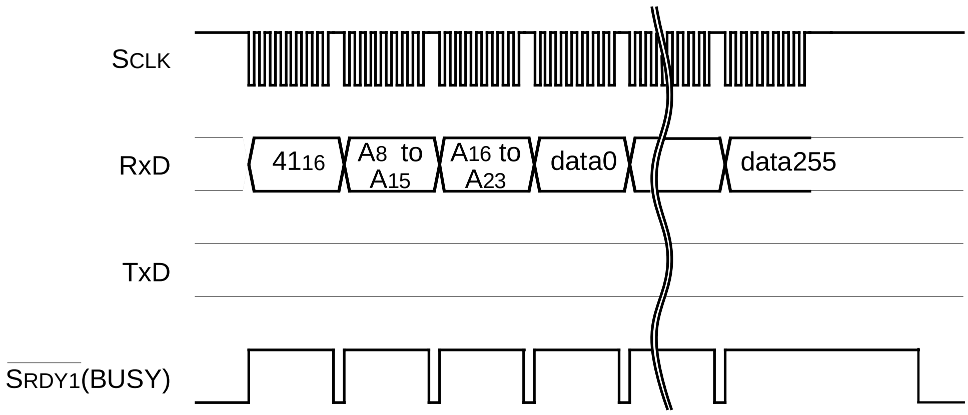


Fig. 60 Timing for the page program

Erase All Blocks Command

This command erases the content of all blocks. Execute the erase all blocks command as explained here following.

(1) Transfer the “$A7_{16}$” command code with the 1st byte.

(2) Transfer the verify command code “$D0_{16}$” with the 2nd byte. With the verify command code, the erase operation will start and continue for all blocks in the flash memory.
When block erasing ends, the $\overline{\text{SRDY1}}$ (BUSY) signal changes from the “H” to the “L” level . The result of the erase operation can be known by reading the status register.

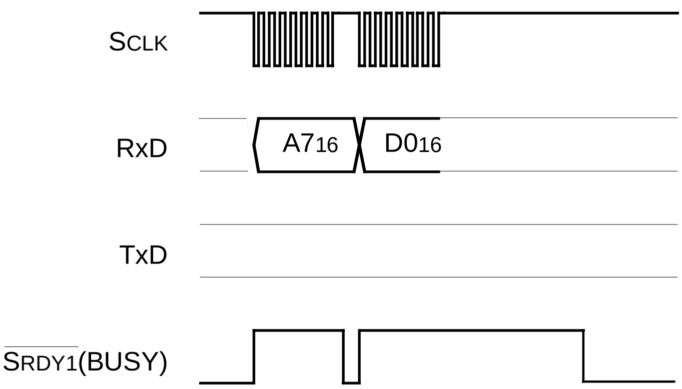


Fig. 61 Timing for erasing all blocks

Download Command

This command downloads a program to the RAM for execution. Execute the download command as explained here following.

(1) Transfer the "FA16" command code with the 1st byte.
(2) Transfer the program size with the 2nd and 3rd bytes.
(3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
(4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.

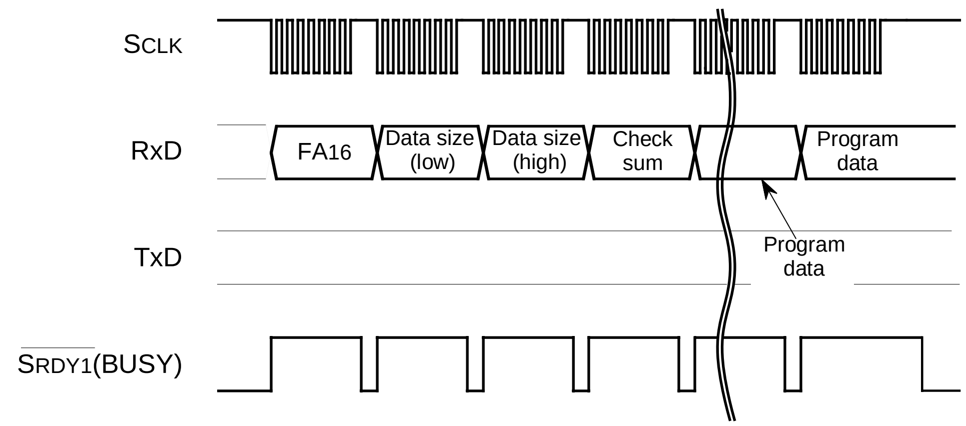


Fig. 62 Timing for download

Version Information Output Command

This command outputs the version information of the control program stored in the boot area. Execute the version information output command as explained here following.

(1) Transfer the "FB16" command code with the 1st byte.
(2) The version information will be output from the 2nd byte onward. This data is composed of 8 ASCII code characters.

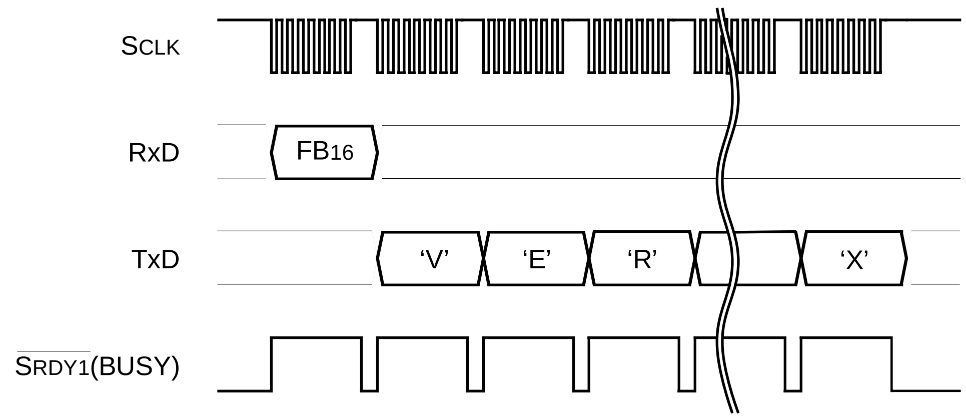


Fig. 63 Timing for version information output

ID Check

This command checks the ID code. Execute the boot ID check command as explained here following.

(1) Transfer the “$F5_{16}$” command code with the 1st byte.

(2) Transfer addresses A_0 to A_7, A_8 to A_{15} and A_{16} to A_{23} (“00_{16}”) of the 1st byte of the ID code with the 2nd, 3rd and 4th bytes respectively.

(3) Transfer the number of data sets of the ID code with the 5th byte.

(4) The ID code is sent with the 6th byte onward, starting with the 1st byte of the code.

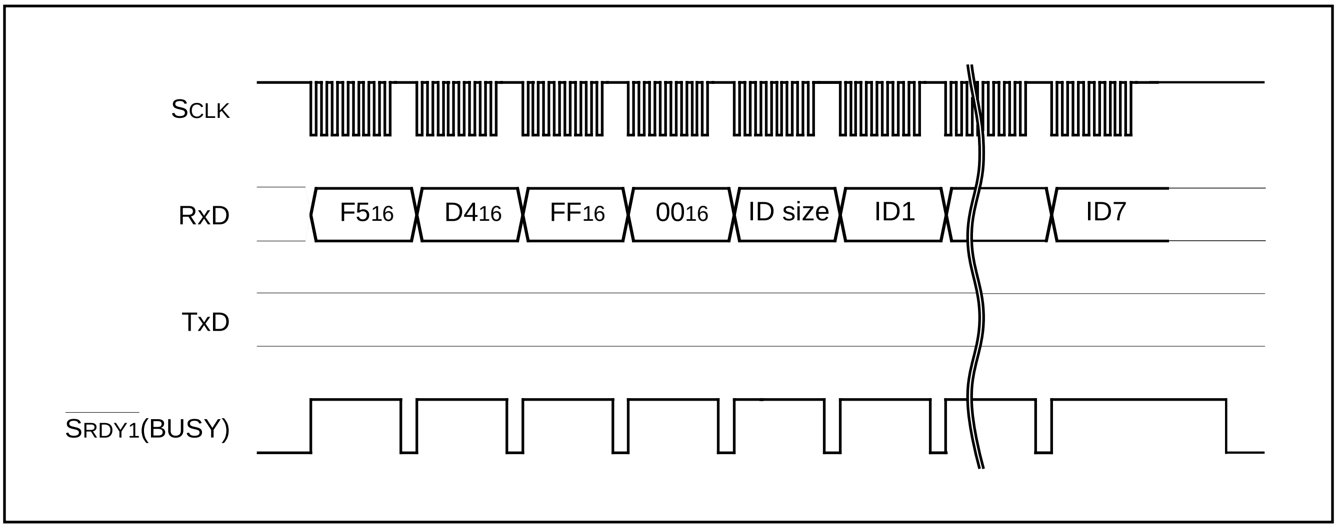


Fig. 64 Timing for the ID check

ID Code

When the flash memory is not blank, the ID code sent from the peripheral units and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the peripheral units is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses $FFD4_{16}$ to $FFDA_{16}$. Write a program into the flash memory, which already has the ID code set for these addresses.

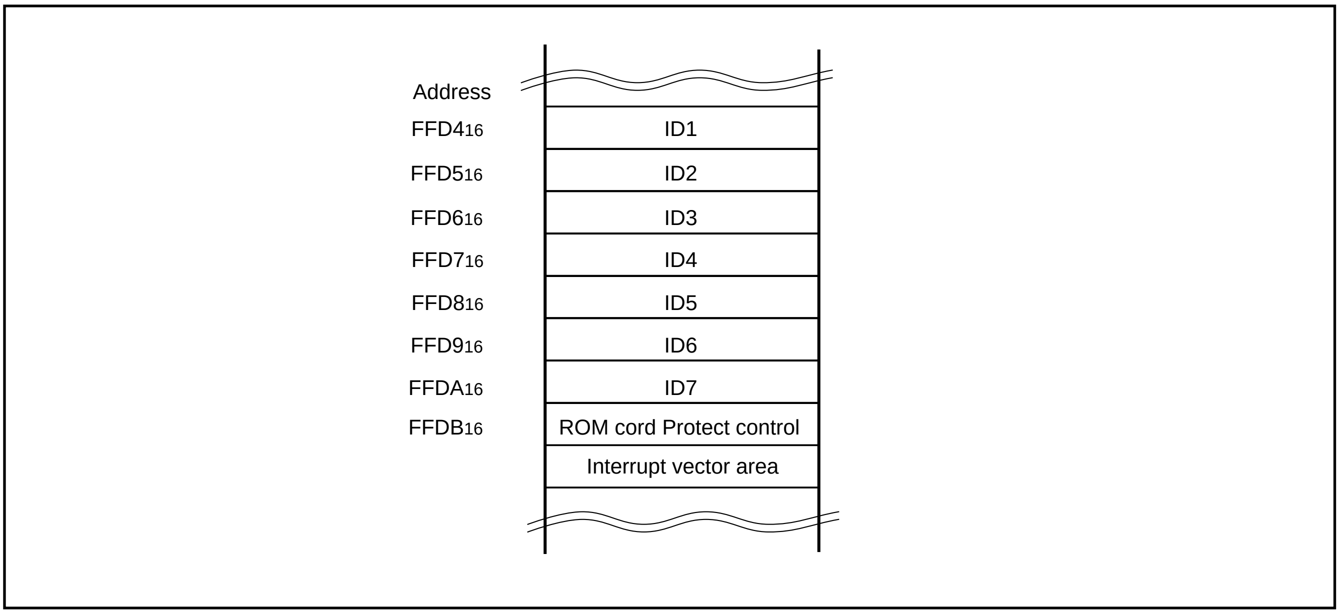


Fig. 65 ID code storage addresses

Status Register (SRD)

The status register indicates operating status of the flash memory and status such as whether an erase operation or a program ended successfully or in error. It can be read by writing the read status register command (70_{16}). Also, the status register is cleared by writing the clear status register command (50_{16}).
Table 18 gives the definition of each status register bit. After clearing the reset, the status register outputs "80_{16}".

Sequencer status (SR7)

After power-on and recover from deep power down mode, the sequencer status is set to "1"(ready).

The sequencer status indicates the operating status of the device. This status bit is set to "0" (busy) during write or erase operation and is set to "1" upon completion of these operations.

Erase Status (SR5)

The erase status reports the operating status of the auto erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

Program Status (SR4)

The program status reports the operating status of the auto write operation. If a write error occurs, it is set to "1". When the program status is cleared, it is set to "0".

Table 18 Status register (SRD)

SRD0 bits	Status name	Definition "1"	Definition "0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

Status Register 1 (SRD1)

Status register 1 indicates the status of serial communications, results from ID checks and results from check sum comparisons. It can be read after the SRD by writing the read status register command (70_{16}). Also, status register 1 is cleared by writing the clear status register command (50_{16}).
Table 19 gives the definition of each status register bit. "00_{16}" is output when power is turned on and the flag status is maintained even after the reset.

Boot Update Completed Bit (SR15)

This flag indicates whether the control program was downloaded to the RAM or not, using the download function.

Check Sum Consistency Bit (SR12)

This flag indicates whether the check sum matches or not when a program is downloaded for execution using the download function.

ID Check Completed Bits (SR11 and SR10)

These flags indicate the result of ID checks. Some commands cannot be accepted without an ID check.

Data Reception Time Out (SR9)

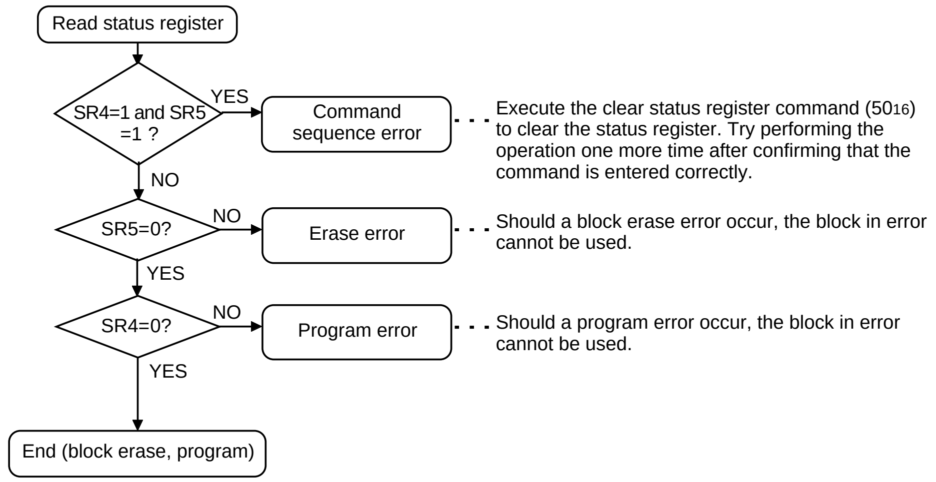
This flag indicates when a time out error is generated during data reception. If this flag is attached during data reception, the received data is discarded and the microcomputer returns to the command wait state.

Table 19 Status register 1 (SRD1)

SRD1 bits	Status name	Definition "1"	Definition "0"
SR15 (bit7)	Boot update completed bit	Update completed	Not Update
SR14 (bit6)	Reserved	-	-
SR13 (bit5)	Reserved	-	-
SR12 (bit4)	Checksum match bit	Match	Mismatch
SR11 (bit3) SR10 (bit2)	ID check completed bits	00 Not verified 01 Verification mismatch 10 Reserved 11 Verified	
SR9 (bit1)	Data reception time out	Time out	Normal operation
SR8 (bit0)	Reserved	-	-

Full Status Check

Results from executed erase and program operations can be known by running a full status check. Figure 66 shows a flowchart of the full status check and explains how to remedy errors which occur.

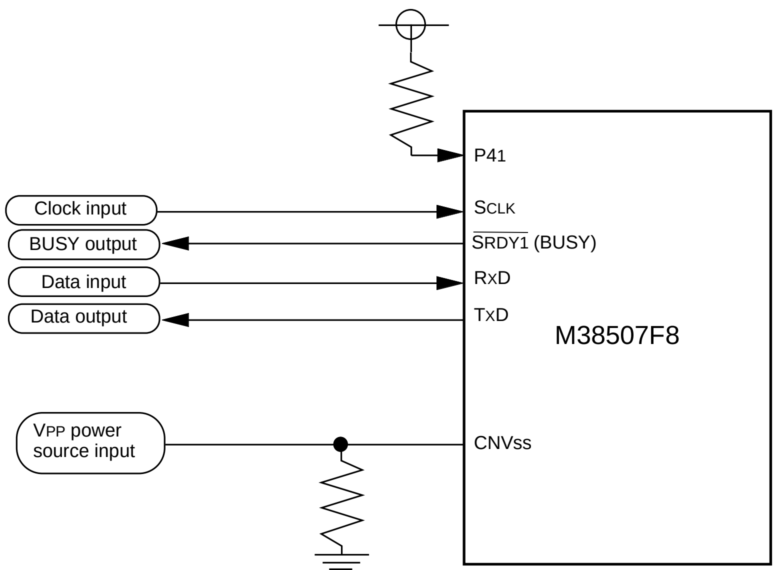


Note: When one of SR5 to SR4 is set to "1", none of the program, erase all blocks commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 66 Full status check flowchart and remedial procedure for errors

Example Circuit Application for The Standard Serial I/O Mode

Figure 67 shows a circuit application for the standard serial I/O mode. Control pins will vary according to programmer, therefore see the peripheral unit manual for more information.



Notes 1: Control pins and external circuitry will vary according to peripheral unit. For more information, see the peripheral unit manual.
2: In this example, the Vpp power supply is supplied from an external source (writer). To use the user's power source, connect to 4.5 V to 5.5 V.

Fig. 67 Example circuit application for the standard serial I/O mode

Flash memory Electrical characteristics

Table 20 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage P0₀–P0₇, P1₀–P1₇, P2₀, P2₁, P2₄–P2₇, P3₀–P3₄, P4₀–P4₄, V_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage P2₂, P2₃		–0.3 to 5.8	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage P0₀–P0₇, P1₀–P1₇, P2₀, P2₁, P2₄–P2₇, P3₀–P3₄, P4₀–P4₄, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage P2₂, P2₃		–0.3 to 5.8	V
P_d	Power dissipation	T_a = 25 °C	1000 (Note)	mW
T_{opr}	Operating temperature		25±5	°C
T_{stg}	Storage temperature		–40 to 125	°C

Note: The rating becomes 300 mW at the 42P2R-A/E package.

Table 21 Flash memory mode Electrical characteristics
(T_a = 25°C, V_{CC} = 4.5 to 5.5V unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{PP1}	V_{PP} power source current (read)	$V_{PP} = V_{CC}$			100	µA
I_{PP2}	V_{PP} power source current (program)	$V_{PP} = V_{CC}$			60	mA
I_{PP3}	V_{PP} power source current (erase)	$V_{PP} = V_{CC}$			30	mA
V_{IL}	“L” input voltage (Note)		0		0.8	V
V_{IH}	“H” input voltage (Note)		2.0		V_{CC}	V
V_{PP}	V_{PP} power source voltage		4.5		5.5	V
V_{CC}	V_{CC} power source voltage	Microcomputer mode operation at V_{CC} = 2.7 to 5.5V	4.5		5.5	V
		Microcomputer mode operation at V_{CC} = 2.7 to 3.6V	3.0		3.6	V

Note: Input pins for parallel I/O mode.

AC Electrical characteristics
(Ta = 25°C, V_{CC} = 4.5 to 5.5V unless otherwise noted)

Table 22 Read-only mode

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{RC}	Read cycle time	200			ns
$t_{a(AD)}$	Address access time			100	ns
$t_{a(CE)}$	$\overline{CE}$ access time			100	ns
$t_{a(OE)}$	$\overline{OE}$ access time			80	ns
t_{CLZ}	Output enable time (after $\overline{CE}$)	0			ns
$t_{DF(CE)}$	Output floating time (after $\overline{CE}$)			25	ns
t_{OLZ}	Output enable time (after $\overline{OE}$)	0			ns
$t_{DF(OE)}$	Output floating time (after $\overline{OE}$)			25	ns
t_{PHZ}	Output floating time (after $\overline{PR}$)			300	ns
t_{OH}	Output valid time (after $\overline{CE}$, $\overline{OE}$, address)	0			ns
t_{OEH}	Write recovery time (before read)	200			ns
t_{PS}	$\overline{RP}$ recovery time	10			µs

Note : Timing measurement condition is showed in Figure 71.

Table 23 Read / Write mode ($\overline{WE}$ control)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WC}	Write cycle time	200			ns
t_{AS}	Address set up time	100			ns
t_{AH}	Address hold time	25			ns
t_{DS}	Data set up time	100			ns
t_{DH}	Data hold time	25			ns
t_{CS}	$\overline{CE}$ set up time	0			ns
t_{CH}	$\overline{CE}$ hold time	0			ns
t_{WP}	$\overline{WE}$ pulse width	100			ns
t_{WPH}	“H” write pulse width	50			ns
t_{DAP}	Program time		25		µs
t_{DAE}	Erase all blocks time		1.5		s
t_{WHRL}	RY/$\overline{BY}$ delay time			200	ns
t_{PS}	$\overline{RP}$ recovery time	10			µs

Note : The read timing parameter in the command write operation mode is same as that of the read-only mode.
Typical value is at V_{CC} = 5.0 V, Ta = 25 °C condition.

Flash memory mode Electrical characteristics
(Ta = 25°C, V_{CC} = 4.5 to 5.5V unless otherwise noted)

Table 24 Read / Write mode ($\overline{CE}$ control)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WC}	Write cycle time	200			ns
t_{AS}	Address set up time	100			ns
t_{AH}	Address hold time	25			ns
t_{DS}	Data set up time	100			ns
t_{DH}	Data hold time	25			ns
t_{WS}	$\overline{WE}$ set up time	0			ns
t_{WH}	$\overline{WE}$ hold time	0			ns
t_{CEP}	$\overline{CE}$ pulse width	100			ns
t_{CEPH}	“H” $\overline{CE}$ pulse width	50			ns
t_{DAP}	Program time		25		µs
t_{DAE}	Erase all blocks time		1.5		s
t_{EHRL}	RY/$\overline{BY}$ delay time			200	ns
t_{PS}	$\overline{RP}$ recovery time	10			µs

Note : The read timing parameter in the command write operation mode is same as that of the read-only mode.
Typical value is at V_{CC} = 5.0 V, Ta = 25 °C condition.

Table 25 Erase and program operation

Parameter	Min.	Typ.	Max.	Unit
Erase all blocks time		1.5		s
Block erase time		1.0		s
Program time (1byte)		25		µs

Table 26 V_{CC} power up / power down timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{VCS}	$\overline{RP}$ = V_{IH} set up time (after rised V_{CC} = V_{CC} min.)	10			µs

Note : Miserase or miswrite may happen, in case of noise pulse due to the power supply on or off is input to the control pins. Therefore disableing the write mode is need for prevent from memory data break at the power supply on or off. 10µs (min.) waiting time is need to initiate read or write operation after V_{CC} rises to V_{CC} min. at power supply on. The memory data is protected owing to keep the $\overline{RP}$ pin V_{IL} level at power supply off. The $\overline{RP}$ pin must be kept V_{IL} level for 10µs (min.) after V_{CC} rises to V_{CC} min. at the power supply on. The $\overline{RP}$ pin must be kept V_{IL} level until the V_{CC} falls to the GND level at power supply off. $\overline{RP}$ pin doesn't have latch mode, so $\overline{RP}$ pin must be kept V_{IH} level during read, erase and program operation.

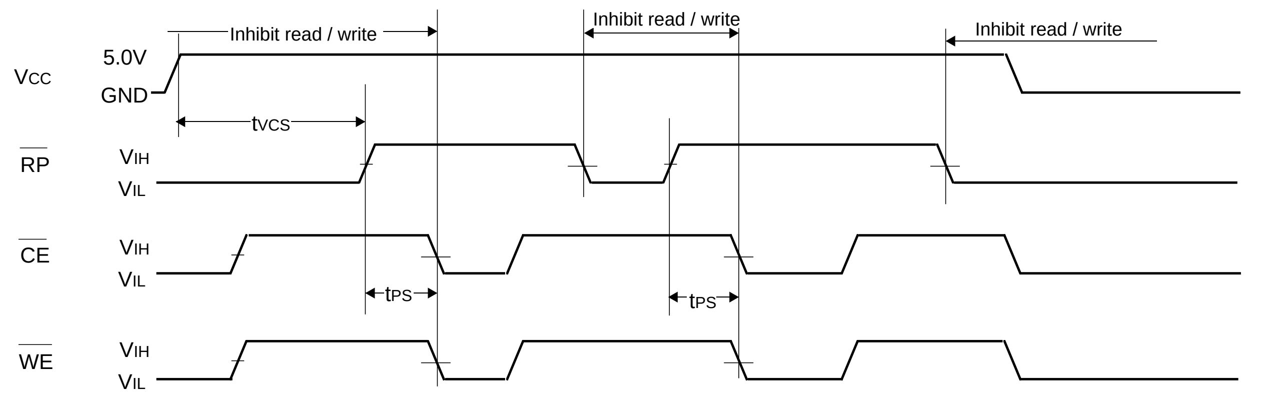


Fig. 68 VCC power up / power down timing

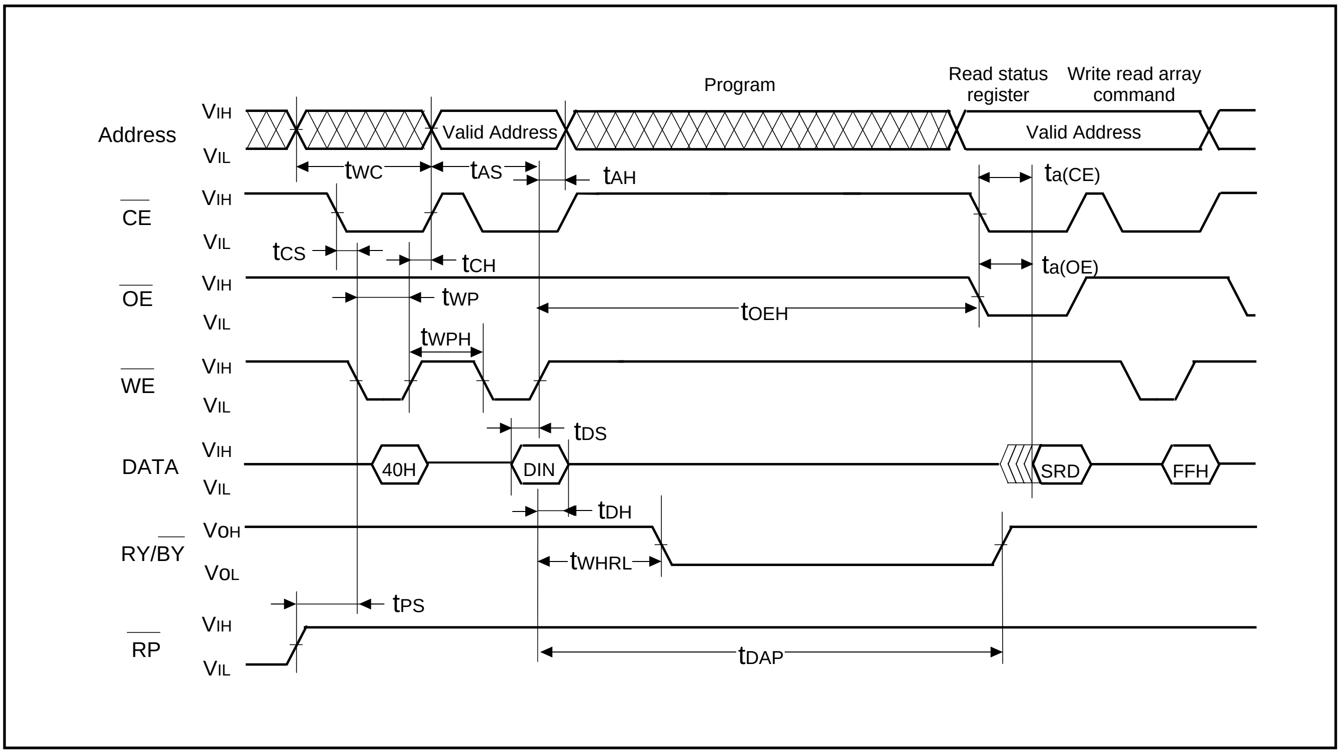


Fig. 69 AC wave for program operation ($\overline{WE}$ control)

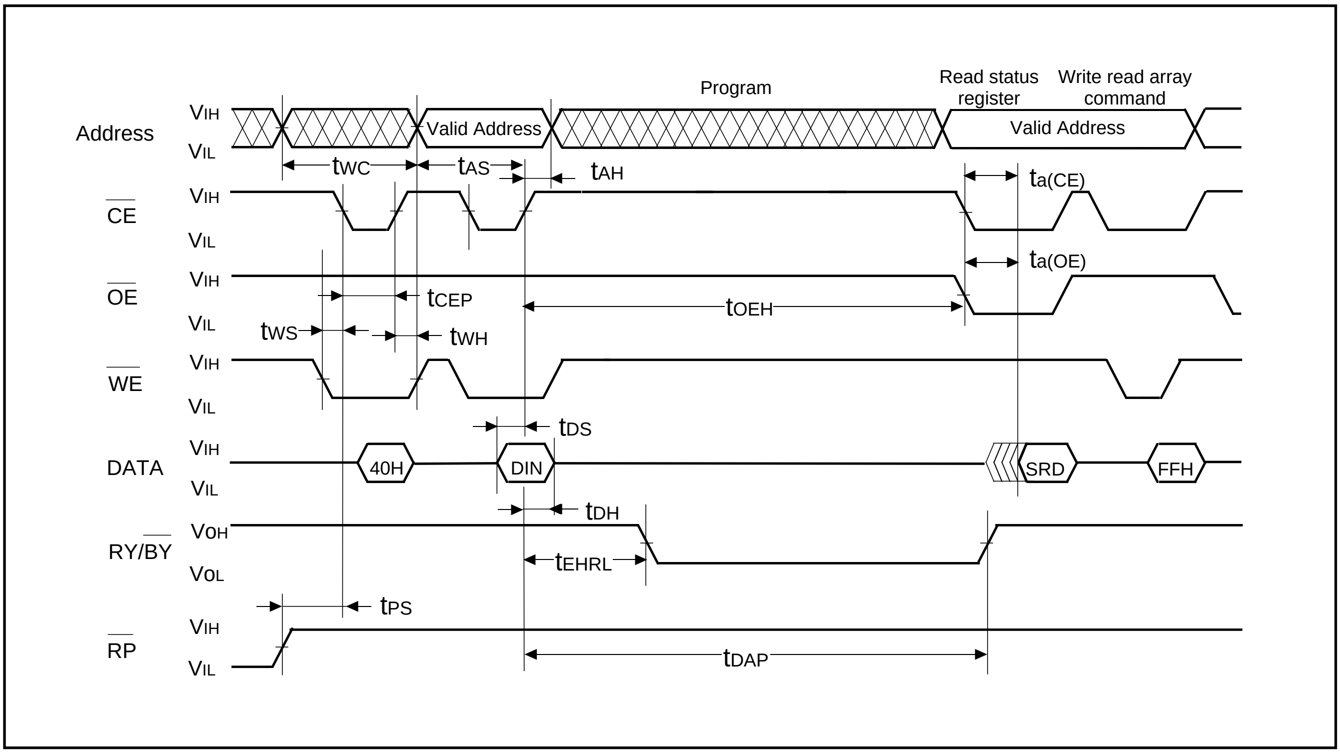


Fig. 70 AC wave for program operation ($\overline{CE}$ control)

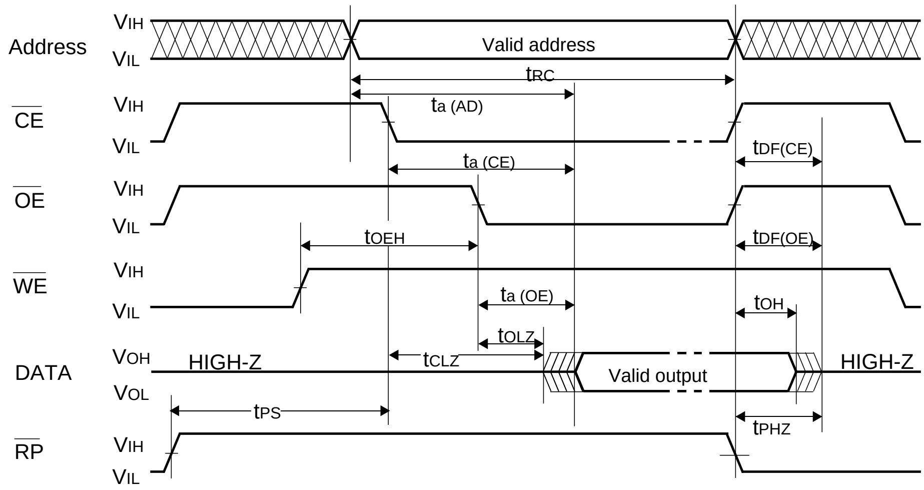
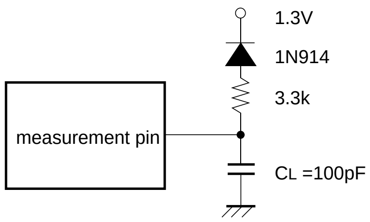


Fig. 71 AC wave for read operation and test condition



AC electrical characteristics test condition

Input voltage : V_{IL} = 0V, V_{IH} = 5.0V
Input signal rising time, falling time : 10ns

Timing measurement
Reference voltage : 1.5V

Load circuit : 1TTL gate+
CL(100pF)

or

Fig. 72 AC electrical characteristics test condition

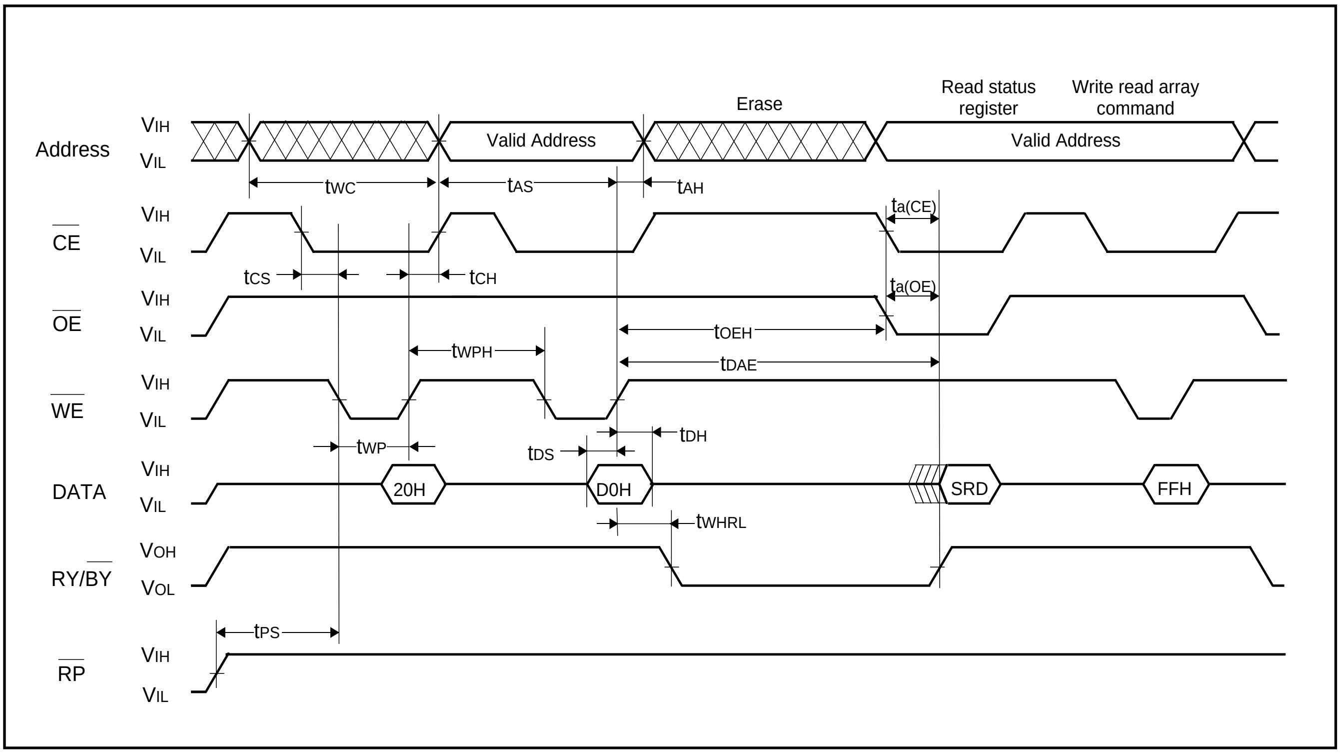


Fig. 73 AC wave for erase operation (WE control)

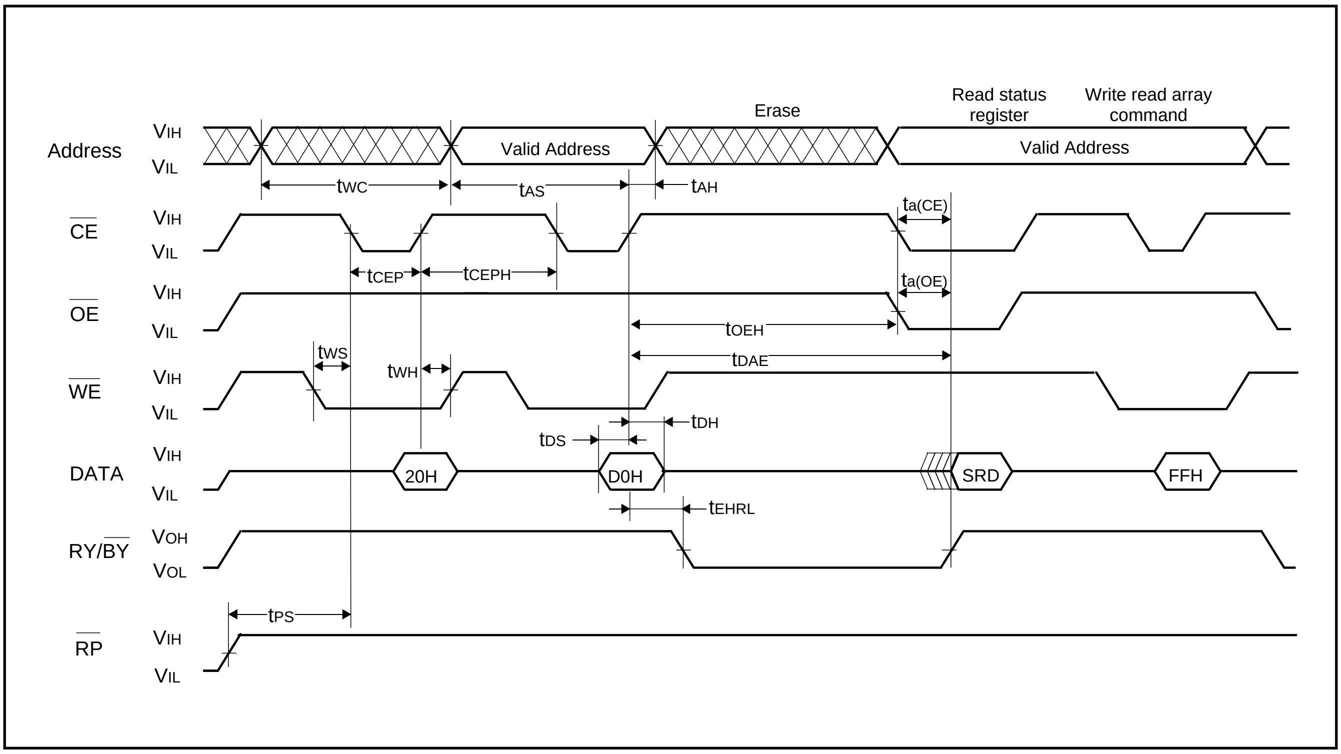


Fig. 74 AC wave for erase operation (CE control)

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1.” After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY1}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY1}}$ output enable bit to “1.”

Serial I/O1 continues to output the final bit from the TxD pin after transmission is completed.

S_{OUT2} pin for serial I/O2 goes to high impedance after transmission is completed.

When an external clock is used as synchronous clock in serial I/O1 or serial I/O2, write transmission data to the transmit buffer register or serial I/O2 register while the transfer clock is “H.”

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that $f(X_{IN})$ in the middle/high-speed mode is at least on 500 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the X_{IN} frequency in high-speed mode.

NOTES ON USAGE

Differences between 3850 group (standard) and 3850 group (spec. H)

(1) The absolute maximum ratings of 3850 group (spec. H) is smaller than that of 3850 group (standard).
- Power source voltage Vcc = –0.3 to 6.5 V
- CNVss input voltage V_I = –0.3 to Vcc +0.3 V

(2) The oscillation circuit constants of X_{IN}-X_{OUT}, X_{CIN}-X_{COUT} may be some differences between 3850 group (standard) and 3850 group (spec. H).

(3) Do not write any data to the reserved area and the reserved bit. (Do not change the contents after rest.)

(4) Fix bit 3 of the CPU mode register to “1”.

(5) Be sure to perform the termination of unused pins.

Handling of Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin) and between power source pin (V_{CC} pin) and analog power source input pin (AV_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF–0.1µF is recommended.

EPROM Version/One Time PROM Version/ Flash Memory Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.

To improve the noise reduction, connect a track between CNVss pin and Vss pin or Vcc pin with 1 to 10 kΩ resistance.

The mask ROM version track of CNVss pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form[*1]
2. Mark Specification Form[*2]
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

DATA REQUIRED FOR One Time PROM PROGRAMMING ORDERS

The following are necessary when ordering a PROM programming service:

1. ROM Programming Confirmation Form[*1]
2. Mark Specification Form[*2] (only special mark with customer's trade mark logo)
3. Data to be programmed to PROM, in EPROM form (three identical copies) or one floppy disk.

For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage.

✻1 Mask ROM Confirmation Forms
http://www.infomicom.mesc.co.jp/38000/38ordere.htm

✻2 Mark Specification Forms
http://www.infomicom.mesc.co.jp/mela/markform.htm

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and buit-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 27 Programming adapter

Package	Name of Programming Adapter
42P4B, 42S1B	PCA4738S-42A
42P2R-A/E	PCA4738F-42A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 75 is recommended to verify programming.

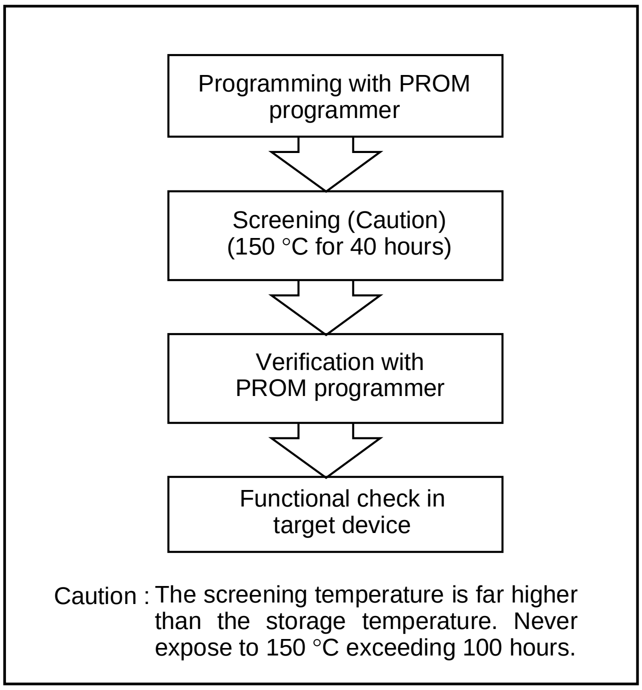


Fig. 75 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Table 28 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage		–0.3 to 6.5	V
V_I	Input voltage P0₀–P0₇, P1₀–P1₇, P2₀, P2₁, P2₄–P2₇, P3₀–P3₄, P4₀–P4₄, V_{REF}	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to V_{CC} +0.3	V
V_I	Input voltage P2₂, P2₃		–0.3 to 5.8	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage P0₀–P0₇, P1₀–P1₇, P2₀, P2₁, P2₄–P2₇, P3₀–P3₄, P4₀–P4₄, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage P2₂, P2₃		–0.3 to 5.8	V
P_d	Power dissipation	T_a = 25 °C	1000 **(Note)**	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Note : The rating becomes 300mW at the 42P2R-A/E package.

Table 29 Recommended operating conditions (1)
(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage	8 MHz (high-speed mode)	4.0	5.0	5.5	V
		8 MHz (middle-speed mode), 4 MHz (high-speed mode)	2.7	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	A-D convert reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage	AN_0–AN_4	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	P0₀–P0₇, P1₀–P1₇, P2₀–P2₇, P3₀–P3₄, P4₀–P4₄	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$, X_{IN}, CNV_{SS}	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage	P0₀–P0₇, P1₀–P1₇, P2₀–P2₇, P3₀–P3₄, P4₀–P4₄	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	$\overline{RESET}$, CNV_{SS}	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage	X_{IN}	0		$0.16V_{CC}$	V
$\Sigma I_{OH(peak)}$	"H" total peak output current	P0₀–P0₇, P1₀–P1₇, P3₀–P3₄ **(Note)**			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	P2₀, P2₁, P2₄–P2₇, P4₀–P4₄ **(Note)**			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note)**	P0₀–P0₇, P3₀–P3₄			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note)**	P1₀–P1₇			120	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	P2₀–P2₇,P4₀–P4₄ **(Note)**			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	P0₀–P0₇, P1₀–P1₇, P3₀–P3₄ **(Note)**			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	P2₀, P2₁, P2₄–P2₇, P4₀–P4₄ **(Note)**			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note)**	P0₀–P0₇, P3₀–P3₄			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note)**	P1₀–P1₇			60	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	P2₀–P2₇,P4₀–P4₄ **(Note)**			40	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 30 Recommended operating conditions (2)
(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ **(Note 1)**			–10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 1)**	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$			10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 1)**	$P1_0$–$P1_7$			20	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ **(Note 2)**			–5	mA
$I_{OL(avg)}$	"L" average output current **(Note 2)**	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$			5	mA
$I_{OL(avg)}$	"L" average output current **(Note 2)**	$P1_0$–$P1_7$			15	mA
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC} = 4.0 to 5.5V) **(Note 3)**				8	MHz
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC} = 2.7 to 5.5V) **(Note 3)**				4	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50%.

Table 31 Electrical characteristics (1)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ **(Note)**	I_{OH} = –10 mA, V_{CC} = 4.0–5.5 V	V_{CC}–2.0			V
		I_{OH} = –1.0 mA, V_{CC} = 2.7–5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$	I_{OL} = 10 mA, V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 1.0 mA, V_{CC} = 2.7–5.5 V			1.0	V
V_{OL}	"L" output voltage $P1_0$–$P1_7$	I_{OL} = 20 mA, V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 10 mA, V_{CC} = 2.7–5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0–INT_3			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD, S_{CLK}			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$			0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_4$, $P4_0$–$P4_4$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4		µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V

Note: $P2_5$ is measured when the $P2_5$/T_XD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".

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Table 32 Electrical characteristics (2)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			6.8	13	mA
		High-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			1.6		mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”	Except M38507F8FP/SP		60	200	µA
			M38507F8FP/SP		T.B.D.		µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			20	40	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”	Except M38507F8FP/SP		20	55	µA
			M38507F8FP/SP		T.B.D.		µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			5.0	10.0	µA
		Middle-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = stopped Output transistors “off”			4.0	7.0	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			1.5		mA
		Increment when A-D conversion is executed $f(X_{IN})$ = 8 MHz			800		µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Table 33 A-D converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 8 MHz, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
–	Resolution					10	bit
–	Absolute accuracy (excluding quantization error)					±4	LSB
t_{CONV}	Conversion time		High-speed mode, Middle-speed mode			61	2tc(X_{IN})
			Low-speed mode		40		µs
R_{LADDER}	Ladder resistor				35		kΩ
I_{VREF}	Reference power source input current	V_{REF} "on"	V_{REF} = 5.0 V	50	150	200	µA
		V_{REF} "off"				5.0	
$I_{I(AD)}$	A-D port input current				0.5	5.0	µA

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TIMING REQUIREMENTS

Table 34 Timing requirements (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	20			X_{IN} cycle
$t_C(X_{IN})$	External clock input cycle time	125			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	50			ns
$t_C(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	80			ns
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	80			ns
$t_{WH}(INT)$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{WL}(INT)$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_C(S_{CLK1})$	Serial I/O1 clock input cycle time **(Note)**	800			ns
$t_{WH}(S_{CLK1})$	Serial I/O1 clock input “H” pulse width **(Note)**	370			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock input “L” pulse width **(Note)**	370			ns
$t_{su}(R_XD-S_{CLK1})$	Serial I/O1 input setup time	220			ns
$t_h(S_{CLK1}-R_XD)$	Serial I/O1 input hold time	100			ns
$t_C(S_{CLK2})$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su}(S_{IN2}-S_{CLK2})$	Serial I/O2 clock input setup time	200			ns
$t_h(S_{CLK2}-S_{IN2})$	Serial I/O2 clock input hold time	200			ns

Note : When $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

Table 35 Timing requirements (2)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\overline{RESET})$	Reset input “L” pulse width	20			X_{IN} cycle
$t_C(X_{IN})$	External clock input cycle time	250			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	100			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	100			ns
$t_C(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	230			ns
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	230			ns
$t_{WH}(INT)$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{WL}(INT)$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_C(S_{CLK1})$	Serial I/O1 clock input cycle time **(Note)**	2000			ns
$t_{WH}(S_{CLK1})$	Serial I/O1 clock input “H” pulse width **(Note)**	950			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock input “L” pulse width **(Note)**	950			ns
$t_{su}(R_XD-S_{CLK1})$	Serial I/O1 input setup time	400			ns
$t_h(S_{CLK1}-R_XD)$	Serial I/O1 input hold time	200			ns
$t_C(S_{CLK2})$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su}(S_{IN2}-S_{CLK2})$	Serial I/O2 clock input setup time	400			ns
$t_h(S_{CLK2}-S_{IN2})$	Serial I/O2 clock input hold time	300			ns

Note : When $f(X_{IN})$ = 4 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when $f(X_{IN})$ = 4 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

Table 36 Switching characteristics (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (SCLK1)	Serial I/O1 clock output "H" pulse width	Fig.76	t_C(SCLK1)/2–30			ns
t_{WL} (SCLK1)	Serial I/O1 clock output "L" pulse width		t_C(SCLK1)/2–30			ns
t_d (SCLK1-TXD)	Serial I/O1 output delay time **(Note 1)**				140	ns
t_v (SCLK1-TXD)	Serial I/O1 output valid time **(Note 1)**		–30			ns
t_r (SCLK1)	Serial I/O1 clock output rising time				30	ns
t_f (SCLK1)	Serial I/O1 clock output falling time				30	ns
t_{WH} (SCLK2)	Serial I/O2 clock output "H" pulse width		t_C(SCLK2)/2–160			ns
t_{WL} (SCLK2)	Serial I/O2 clock output "L" pulse width		t_C(SCLK2)/2–160			ns
t_d (SCLK2-SOUT2)	Serial I/O2 output delay time **(Note 2)**				200	ns
t_v (SCLK2-SOUT2)	Serial I/O2 output valid time **(Note 2)**		0			ns
t_f (SCLK2)	Serial I/O2 clock output falling time				30	ns
t_r (CMOS)	CMOS output rising time **(Note 3)**			10	30	ns
t_f (CMOS)	CMOS output falling time **(Note 3)**			10	30	ns

Notes 1: When the P2₅/TXD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: When the P0₁/SOUT2 and P0₂/SCLK2 P-channel output disable bit of the Serial I/O2 control register 1 (bit 7 of address 0015_{16}) is "0".
3: The XOUT pin is excluded.

Table 37 Switching characteristics (2)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (SCLK1)	Serial I/O1 clock output "H" pulse width	Fig.76	t_C(SCLK1)/2–50			ns
t_{WL} (SCLK1)	Serial I/O1 clock output "L" pulse width		t_C(SCLK1)/2–50			ns
t_d (SCLK1-TXD)	Serial I/O1 output delay time **(Note 1)**				350	ns
t_v (SCLK1-TXD)	Serial I/O1 output valid time **(Note 1)**		–30			ns
t_r (SCLK1)	Serial I/O1 clock output rising time				50	ns
t_f (SCLK1)	Serial I/O1 clock output falling time				50	ns
t_{WH} (SCLK2)	Serial I/O2 clock output "H" pulse width		t_C(SCLK2)/2–240			ns
t_{WL} (SCLK2)	Serial I/O2 clock output "L" pulse width		t_C(SCLK2)/2–240			ns
t_d (SCLK2-SOUT2)	Serial I/O2 output delay time **(Note 2)**				400	ns
t_v (SCLK2-SOUT2)	Serial I/O2 output valid time **(Note 2)**		0			ns
t_f (SCLK2)	Serial I/O2 clock output falling time				50	ns
t_r (CMOS)	CMOS output rising time **(Note 3)**			20	50	ns
t_f (CMOS)	CMOS output falling time **(Note 3)**			20	50	ns

Notes 1: When the P2₅/TXD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: When the P0₁/SOUT2 and P0₂/SCLK2 P-channel output disable bit of the Serial I/O2 control register 1 (bit 7 of address 0015_{16}) is "0".
3: The XOUT pin is excluded.

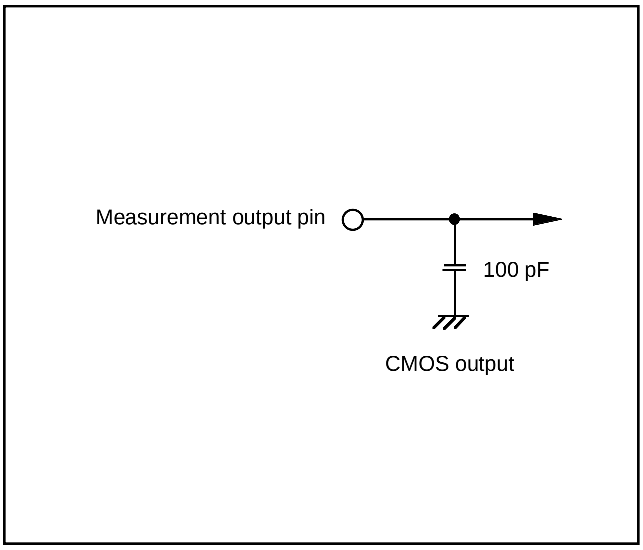


Fig. 76 Circuit for measuring output switching characteristics

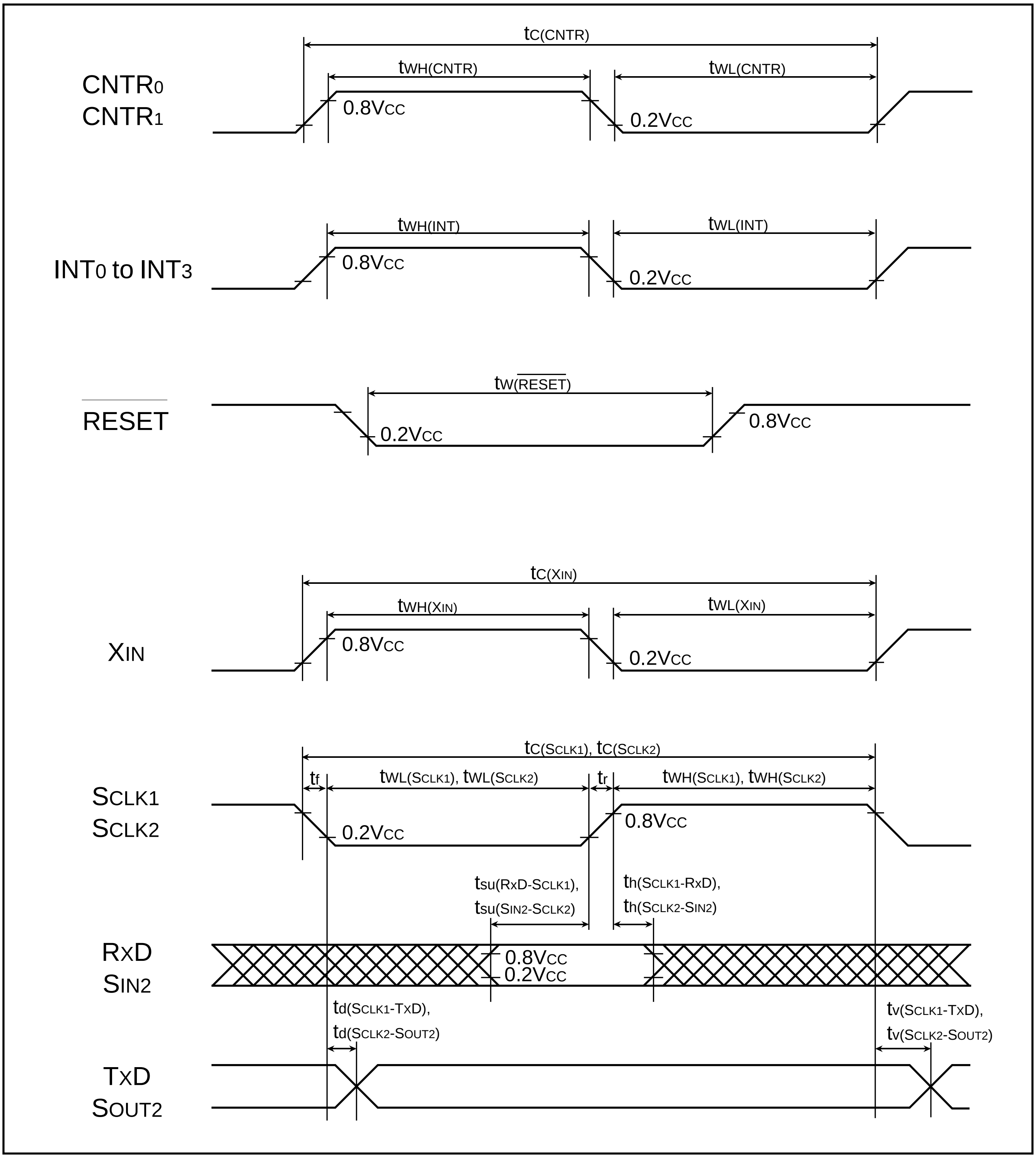


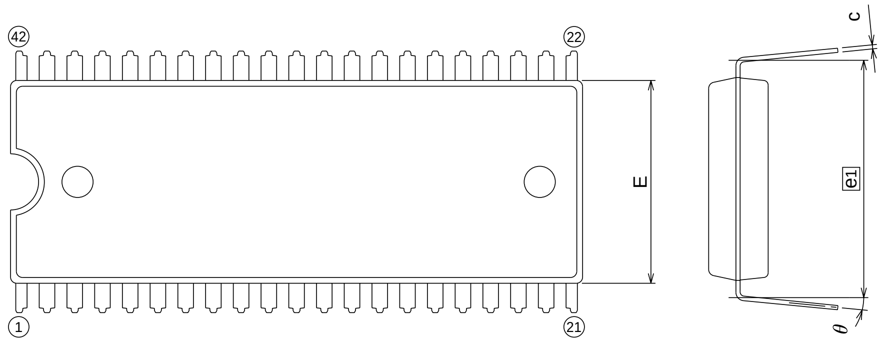
Fig. 77 Timing diagram

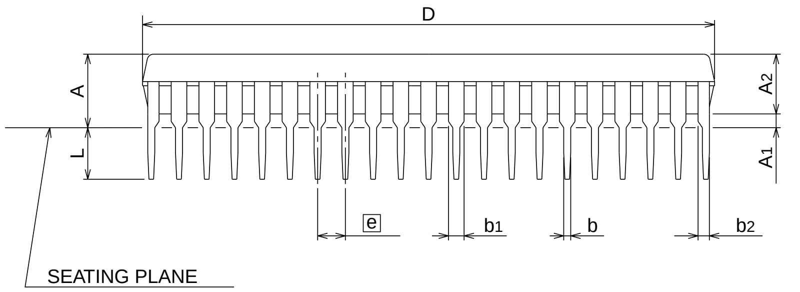
PACKAGE OUTLINE

42P4B

Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	–	4.1	Alloy 42/Cu Alloy



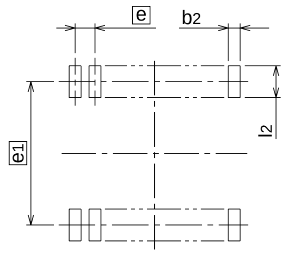


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	–	1.778	–
e_1	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

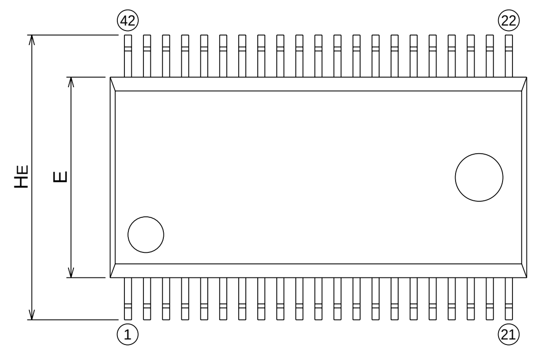
42P2R-A/E

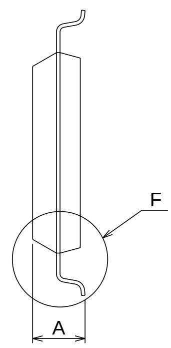
Plastic 42pin 450mil SSOP

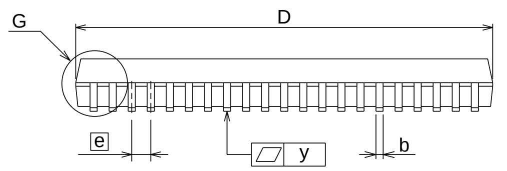
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	–	0.63	Alloy 42

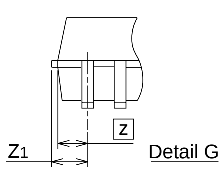


Recommended Mount Pad

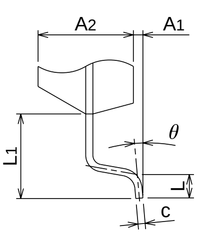








Detail G



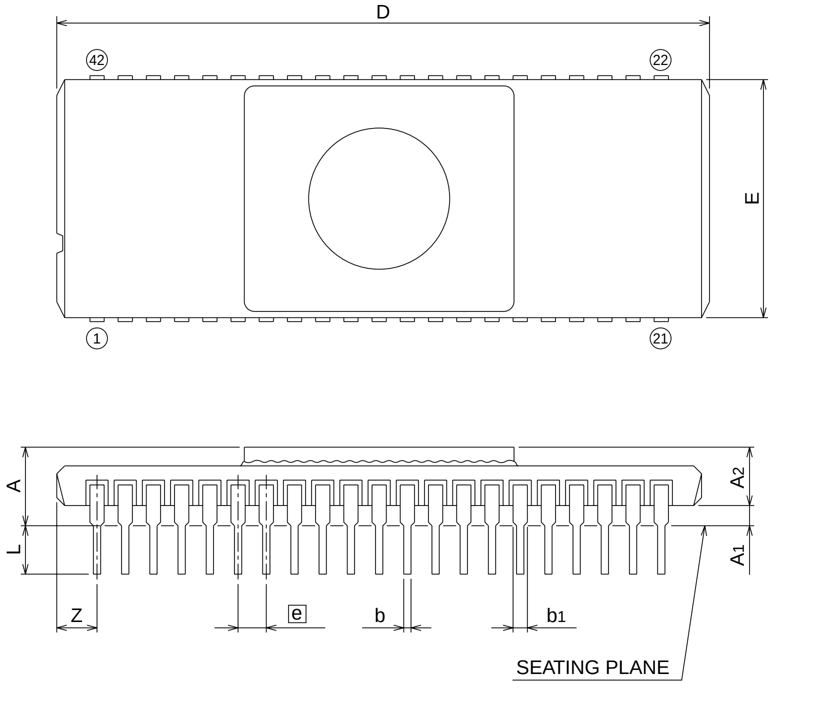
Detail F

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	0.8	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
z	–	0.75	–
Z_1	–	–	0.9
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.5	–
e_1	–	11.43	–
I_2	1.27	–	–

42S1B-A

Metal seal 42pin 600mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
WDIP42-C-600-1.78	–	



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.0
A_1	1.0	–	–
A_2	–	–	3.44
b	0.38	0.46	0.54
b_1	0.7	0.8	0.9
c	0.17	0.25	0.33
D	–	–	41.1
E	–	–	15.8
e	–	1.778	–
e_1	–	15.24	–
L	3.05	–	–
Z	–	–	3.05

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE: 2-2-3, MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN

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1.0	First Edition	000309
1.1	Font errors are revised.	000322
2.0	Page 1; "●Interrupts" of "FEATURES" is revised. Page 1; Figure 1 is partly revised. Page 6; Table 3 is partly revised. Page 17; Explanations of "INTERRUPTS" are partly revised. Page 23; Figure 20 is partly revised. Page 27; Figure 24 is partly revised. Page 33; Explanations of "RESET CIRCUIT" are partly revised. Page 36; Note 1 into Figure 42 is partly revised. Pages 38 to 71; Explanations of "FLASH MEMORY VERSION" are added. Page 41; Figure 45 is partly revised. Page 72; "EPROM Version/One Time PROM Version/Flash Memory Version" of "NOTES ON USAGE" is added. Page 73; "DATA REQUIRED FOR MASK ORDERS" is added. Page 73; "DATA REQUIRED FOR One Time PROM PROGRAMMING ORDERS" is added. Page 73; "ROM PROGRAMMING METHOD" is added. Page 77; Table 32 is partly revised. Page 79; Limit of tw($\overline{\text{RESET}}$) into Table 34 is revised. Page 79; Limit of tw($\overline{\text{RESET}}$) into Table 35 is revised.	001222